TECHNICAL MANUAL

DIRECT SUPPORT MAINTENANCE MANUAL

TRANSMITTING SET, RADAR DATA

AN/AKT-18B

(NSN 5841-01-070-4408)

HEADQUARTERS, DEPARTMENT OF THE ARMY

MARCH 1981

5 SAFETY STEPS TO FOLLOW IF SOMEONE IS THE VICTIM OF ELECTRICAL SHOCK

1. DO NOT TRY TO PULL OR GRAB THE INDIVIDUAL
2. IF POSSIBLE, TURN OFF THE ELECTRICAL POWER
3. IF YOU CANNOT TURN OFF THE ELECTRICAL POWER, PULL, PUSH OR LIFT THE PERSON TO SAFETY USING A DRY WOODEN POLE OR A DRY ROPE OR SOME OTHER INSULATING MATERIAL
4. SEND FOR HELP AS SOON AS POSSIBLE
5. AFTER THE INJURED PERSON IS FREE OF CONTACT WITH THE SOURCE OF ELECTRICAL SHOCK, MOVE THE PERSON A SHORT DISTANCE AWAY AND IMMEDIATELY START ARTIFICIAL RESUSCITATION

Change
No.1

HEADQUARTERS
DEPARTMENT OF THE ARMY
Washington, DC,1 June 1983

DIRECT SUPPORT MAINTENANCE MANUAL
TRANSMITTING SET, RADAR DATA AN/AKT-18B
(NSN 5841-01-070-4408)

TM 11-5841-287-30, March 1981, is changed as follows

1. New or changed material is indicated by a vertical bar In the margin of the page

2. Added or revised illustrations are indicated by a miniature pointing hand and a vertical bar adjacent to the illustration identification number

3. Remove and insert pages as indicated below

Remove	*Insert*
I and ii	i and ii
1-1	1-1/(1-2 blank)
2-1 and 2-2	2-1 and 2-2
3-1 and 3-2	3-1 and 3-2
3-9 through 3-12	3-9 through 3-12
3-27 and 3-28	3-27 and 3-28
3-31 and 3-32	3-31 and 3-32
3-49 and 3-50	3-49 and 3-50
A-1	A-1/(A-2 blank)
Index-1 and Index-2	Index 1 and Index 2

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WARNING

All operations must conform to TB 385-4, Safety Precautions for Maintenance of Electrical/Electronic Equipment (8 August 1979)

WARNING

Dangerous voltages exist in this equipment Serious injury or DEATH may result from contact with terminals carrying dangerous voltages Make sure all power is off when disassembling this equipment DO NOT service or adjust the equipment alone Always have another person available to give first aid in case of an accident

WARNING

Be aware of the WARNING pertaining to TRICHLOROTRIFLUOROETHANE before doing any work with cleaning compounds or chemicals Before using these agents, check with your local Safety Office or Preventive Medicine Activity They can provide information on any hazards when using these agents and how to avoid them

TECHNICAL MANUAL

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REPORTING ERRORS AND RECOMMENDING IMPROVEMENTS

You can help Improve this manual. If you find any mistakes or if you know of a way to improve the procedures, please let us know. Mail your letter, DA Form 2028 (Recommended Changes to Publications and Blank Forms), or DA Form 2028-2 located In back of this manual direct to: Commander, US Army Communications - Electronics Command and Fort Monmouth, AlTN: DRSEL-ME-MP, Fort Monmouth, New Jersey 07703.Paragrph

In either case, a reply will be furnished direct to you.

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CHAPTER 1

INTRODUCTION

1-1. Scope

This manual contains Instructions and information for use by direct support personnel applicable to Transmitting Set, Radar Data AN/AKT-18B (hereinafter referred to as data transmitting set)

1-2. Consolidated Index of Army Publications and Blank Forms.

Refer to the latest Issue of DA Pam 310-1 to determine whether there are new editions, changes, or additional publications pertaining to the equipment

1-3. Maintenance Forms, Records, and Reports

a. Reports of Maintenance and Unsatisfactory Equipment Department of the Army forms and procedures used for equipment maintenance will be those prescribed by TM 38-750, The Army Maintenance Management System (TAMMS)

b. Report of Packaging and Handling Deficiencies
Fill out and forward SF 364 (Report of Discrepancy (ROD)) as prescribed in AR 735-11-2/DLAR 4140 55/NAVMATINST 4355 73/AFR 400-54/MCO 4430 3E

c. Discrepancy in Shipment Report (DISREP) (SF361) Fill out and forward Discrepancy In Shipment Report (DISREP) (SF 361) as prescribed in AR55-38/NAVSUPINST 4610 33B/AFR 75-18/MCO P4610.19C/DL AR 4500 15

1-4. Reporting Equipment Improvement Recommendations (EIR)

If your data transmitting set needs improvement, let us know Send us an EIR You, the user, are the only one who can tell us what you don't like about your equipment Let us know why you don't like the design Put it on an SF 368 (Quality Deficiency Report) Mail it to Commander, US Army Communications-Electronics Command and Fort Monmouth, ATTN DRSEL-ME-MP, Fort Monmouth, New Jersey 07703 We'll send you a reply

1-5. Description

Table 1-1 lists all major components of the data transmitting set Refer to TM 11-5841-287-12 for a description of the Items listed in table 1-1

Table 1-1. Official Nomenclature Cross Reference List

Official nomenclature	Common name
Transmitting Set, Radar Data AN/AKT-18B	Data transmitting set
Encoder, Video KY-865/AKT-18B	Encoder (unit 2)
Control, Data Lmk C-10546/AKT-18B	Data link control (unit 3)
Mounting Base, Electrical Equipment MT-6016/AKT-18B	Encoder mount
Radio Set AN/ARC- 164(V16	Uhf radio set (unit 1)
Receiver-Transmitter, RADIO RT-1288A/ARC-164(V)	Uhf receiver-transmitter (unit 1A1)
Control, Radio Set C- 10547/A RC- 164(V)	Uhf radio control (unit 1A2)
Mounting Base, Electrical Equipment MT-6017/ARC-164(V)	Uhf radio mount (unit 1A3)
Antenna AT-450/ARC	Uhf antenna (unit 4)

CHAPTER 2

PRINCIPLES OF OPERATION

Section I. OVERALL SYSTEM OPERATION

2-1. General Information

The data transmitting set, when used in conjunction with Radar Surveillance Set AN/APS-94F (radar set), provides near realtime radar imagery transmission to geographically dispersed ground stations The data transmitting set transmits over a frequency range of 225 to 400 MHz, utilizing frequency modulation-frequency shift keying (FM-FSK) carrier modulation The data transmission bit rate is 41 6 kilobits/second and the maximum bandwidth is 60 kHz The data transmitting set receives input data consisting of moving target (MT) and fixed target (FT) radar video signals, radar mode data, and ADAS (airborne data annotation system) data from the associated radar set Before application to the data transmitting set, preprocessing of the MT video data is performed for purposes of extracting the fixed target residue components Re-introduction of FT residue is performed by the ground station, which results in improved residue quality and independent residue control Automatic self testing capability provided by built-in test equipment (BITE) is incorporated in the data transmitting set This feature enables the operator to determine go/no-go status of the system prior to use, as well as facilitating system level maintenance.

2-2. Functional Description
(fig 2-1)

The data transmitting set consists of two main subsystems encoding subsystem and transmitting subsystem Figure 2-1 provides applicable block diagram details.

a. Encoding Subsystem (fig 2-1) The encoding subsystem consists of an encoder and data link control. The encoder receives the MT and FT radar video signals from the radar set, which it processes into digitally encoded serial bit stream The encoder also receives radar mode and ADAS data, which is processed along with the radar video data for incorporation in the serial data stream To accomplish this variety of data processing and encoding, the encoder incorporates automatic data processing circuitry which implements program instructions stored in resident memory The data link control interfaces with the encoder to provide centralized control facilities for operational/BITE mode selection and display facilities for indicating BITE status/results.

*b. Transmitting Subsystem (fig 2-1) The trans*mitting subsystem consists of a uhf receiver-transmitter and uhf radio control The uhf receiver transmitter is used for transmitting encoded data (to the

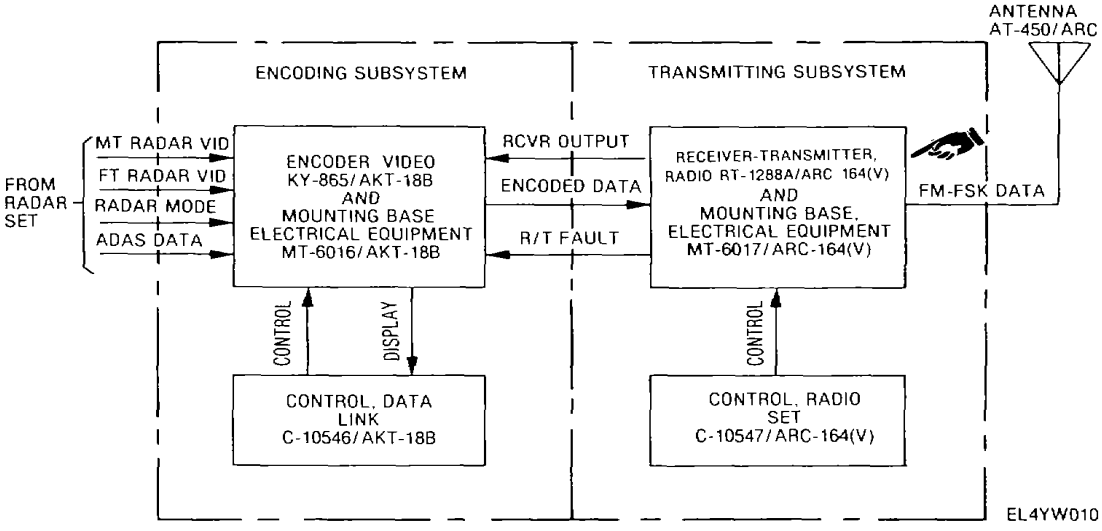


Figure 2-1. Data transmitting set block diagram

ground station) in FM-FSK format, using a carrier deviation of + 12 5kHz A portion of the transmitted output signal is also coupled to the receiver section where it undergoes demodulation The demodulated signal (RCVR OUTPUT) is then returned to the encoder for characteristic evaluation The receiver-transmitter also contains independent self-check circuitry, which automatically supplies a fault signal to the encoder following a synchronization or low rf power malfunction The uhf radio control interfaces with the uhf receiver-transmitter to enable operator channel/frequency selection.

c. BITE Operation BITE encompasses a network of self test circuits, some of which operate on a continuous basis (on-line BITE), while others function only upon operator request (operator initiated BITE). Continuous monitoring of power supply functions is performed within the encoder, while synchronization and low rf power are monitored continuously within the uhf receiver-transmitter In addition, during all data transmitting periods, a demodulated sample of the transmitted signal R/T FAULT is continuously monitored by the encoder for proper data characteristics Two modes of operator initiated BITE are provided airborne and downlink. During airborne BITE, a series of functional tests are performed on the encoder using simulated input data, while the resultant output data is checked for proper data characteristics During downlink BITE, the encoder test sequence is repeated, followed by continuous transmission of a fixed test pattern to the ground station Downlink BITE thus encompasses a complete end-to-end system check In addition, since the exact characteristics of the test pattern are known, the ground station equipment can be adjusted for optimum imagery reproduction, as needed Notification of deleted BITE malfunctions is provided by indicators on the data link control, which also provides the controls for selection of the airborne and downlink BITE modes.

d. Power Distribution and Control (fig. 2-2) Primary power, consisting of 115 V ac, 400 Hz, single phase and 28 V dc, is distributed directly to the encoder and uhf radio mount The uhf radio mount, in turn, distributes the primary power to the uhf receiver-transmitter. Adjustable dc power for edge lighting (0-28 volts) is distributed to the data link control and uhf radio control from the aircraft dc lights control console Application of 115 V ac primary power within the encoder is controlled by the data link control via the 28V CONT PWR line Power control of the uhf receiver-transmitter is accomplished via the data link control STBY and XMT output lines, which, in turn, control the RT PWR ON/OFF and XMT lines outputted by the encoder to the uhf receiver-transmitter In the transmit mode of operation, the RT PWR ON/OFF and XMT signals transition low, in which case the uhf receiver-transmitter is fully energized and is capable of output transmission In the standby mode of operation, XMT is high (22 8 V), in which case the uhf receiver-transmitter Is only partially energized and is incapable of transmission.

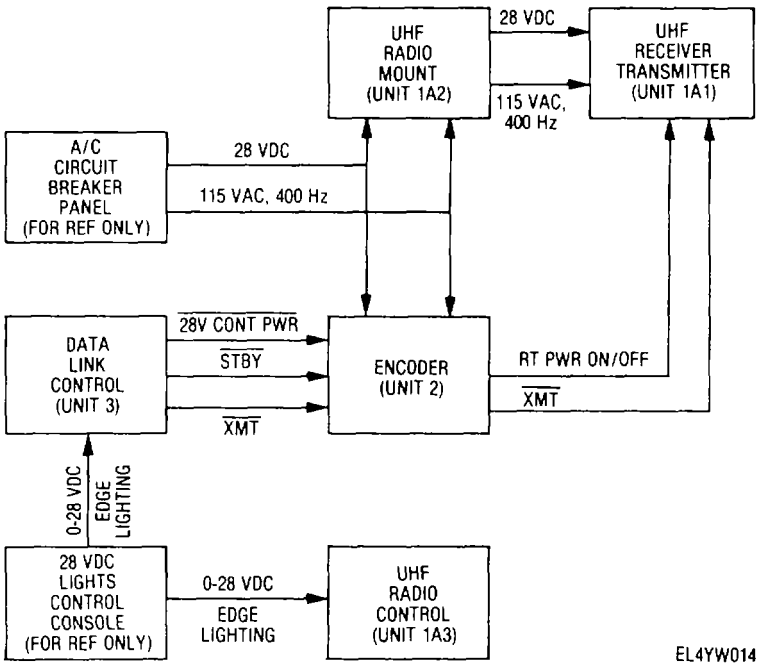


Figure 2-2. System power distribution and control block diagram.

Section II. FUNCTION OF ENCODING SUBSYSTEM

2-3. General

The encoder receives moving target (MT) and fixed target (FT) radar video data, radar mode data and ADAS data, which it processes (encodes) into a single serial data stream suitable for downlink transmission to the ground station The encoded data is structured in frames consisting of 12, 890 bits At a bit rate of 41, 667 bits/second, each frame requires 0 309 second to transmit Because of system bandwidth limitations, video data is grouped into three range fields, designated A, B and C, A-field being closest to the aircraft. Each video field, in turn, is divided into 560 range bins, which represent the smallest unit distance for which separate video data is generated. A-field data is transmitted every frame, while B- and C-field data is transmitted during alternate frames.

2-4. Data Frame Structure

(fig 2-3)

The contents of a typical data frame are illustrated m figure 2-3. The preamble, consisting of 31 bits of fixed code, is the first data to be transmitted. Following the preamble, an 11-bit radar mode word is transmitted. The radar mode word contains such information as ADAS print command, antenna status (left or right), antenna mode (single or both), and video field status (A/B or A/C) Forty-eight 11-bit ADAS data words are transmitted next Certain ADAS navigational data words are replaced by the encoder with equivalent substitute data, which is derived from the radar set recorder The substituted data represents radar range and range delay, aircraft drift angle, and aircraft ground speed The remaining transmitted data consists of 1120, 11-bit words, representing video field data To counteract the effects of a high noise environment, check bits and error correcting codes are incorporated within the data structure (see fig 2-3) In the case of radar mode and ADAS words, three parity bits are provided Protection of FT target data is accomplished by using ID and parity bits, while MT data protection is accomplished by ID and Hamming code bits (para 2-8e)

2-5. Overall Functional Description

(fig 2-4)

The following paragraphs describe overall functional operation of the encoding subsystem Refer to figure 2-4 for applicable block diagram details

a. General Upon entering the encoder, the radar video, radar mode, and ADAS data undergoes conversion to 8-bit parallel format by the input data processing circuitry After conversion to suitable digital form, the data is transferred to the output memory under central processing unit (CPU) control In the case of radar video data, the CPU is bypassed, transfer being direct to the output memory The contents of the output memory are transferred, word-by-word, to the output format generator for final processing During final processing, parity and/or ID bits are added to the various data words, as required Program instructions controlling input data processing, data transfer, and output formatting are permanently stored in the output ROM (read only memory), while the variable radar video, radar mode, and ADAS data are stored in output RAM (random access memory)

b. *Video Input Data Processing* The radar video data signals (MT/FT VIDEO) are processed by dividing each video pulse period into 1680 range units (bins) and generating a digital magnitude word representative of video amplitude for each of the 1680 range bins Magnitude data for each range bin is accumulated over 256 radar pulse repetition intervals (PRI) for A-field and 512 PRI for B- and C-fields An average magnitude value is then computed for each range bin, expressed as an 8-bit data word As a final step, the data is placed on the data bus for transfer to the RAM portion of the output memory Synchronization during video data accumulation is derived from an external 5 MHz gated clock signal (GTD CLOCK) Synchronization during video data transfer is completely asynchronous to video data accumulation and is accomplished using internally generated frequency references The clock rate during video data transfer is 1 25 MHz

c. ADAS *Input Data Processing* The ADAS input data signal (DATA) is received m the form of 48 11-bit data words, each containing two, 4-bit ADAS characters ADAS processing is accomplished simply by loading a serial-ln-parallel-out register with two complete ADAS words (minus parity bits), and then transferring the data words (via the data bus) to output RAM under CPU control This cycle is repeated for each of the 48 ADAS data words Substitute RANGE and RANGE DELAY input data is received in the form of eight binary type signals Two of these signals are used for representation of the three possible radar ranges (25/501100 km), while the remaining signals are used for representation of the seven possible range delay conditions (0110120130/40/50/60 km) Similar to ADAS data, the range and range delay data word is transferred (via the data bus) to output RAM under CPU control

d. *Ground Speed Input Data Processing* Substitute aircraft ground speed data (FILM SPEED) is received in the form of a variable rate pulse stream The higher the ground speed, the higher the pulse rate Conversion of the variable-rate pulse to binary code is accomplished by counting a fixed rate clock between two

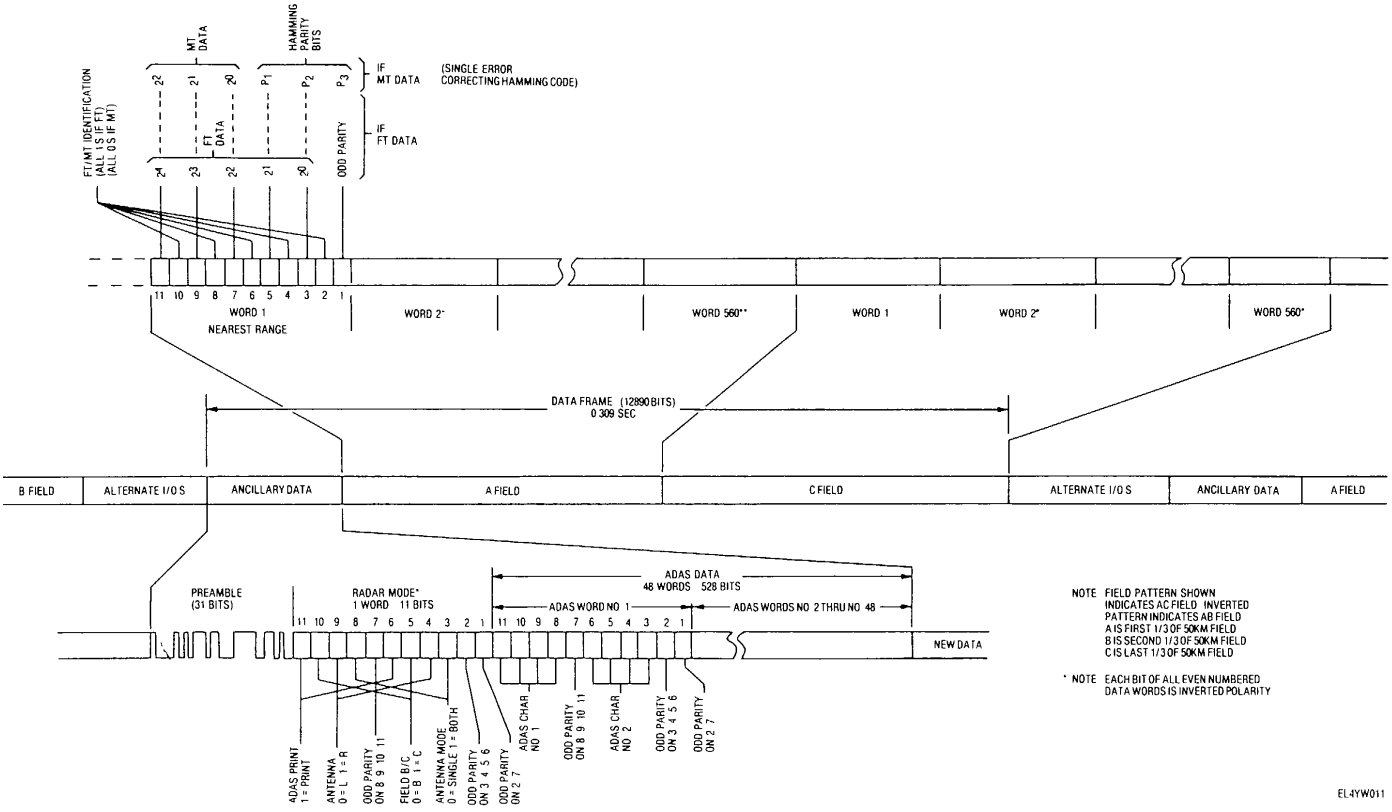


Figure 2-3. Typical data frame structure.

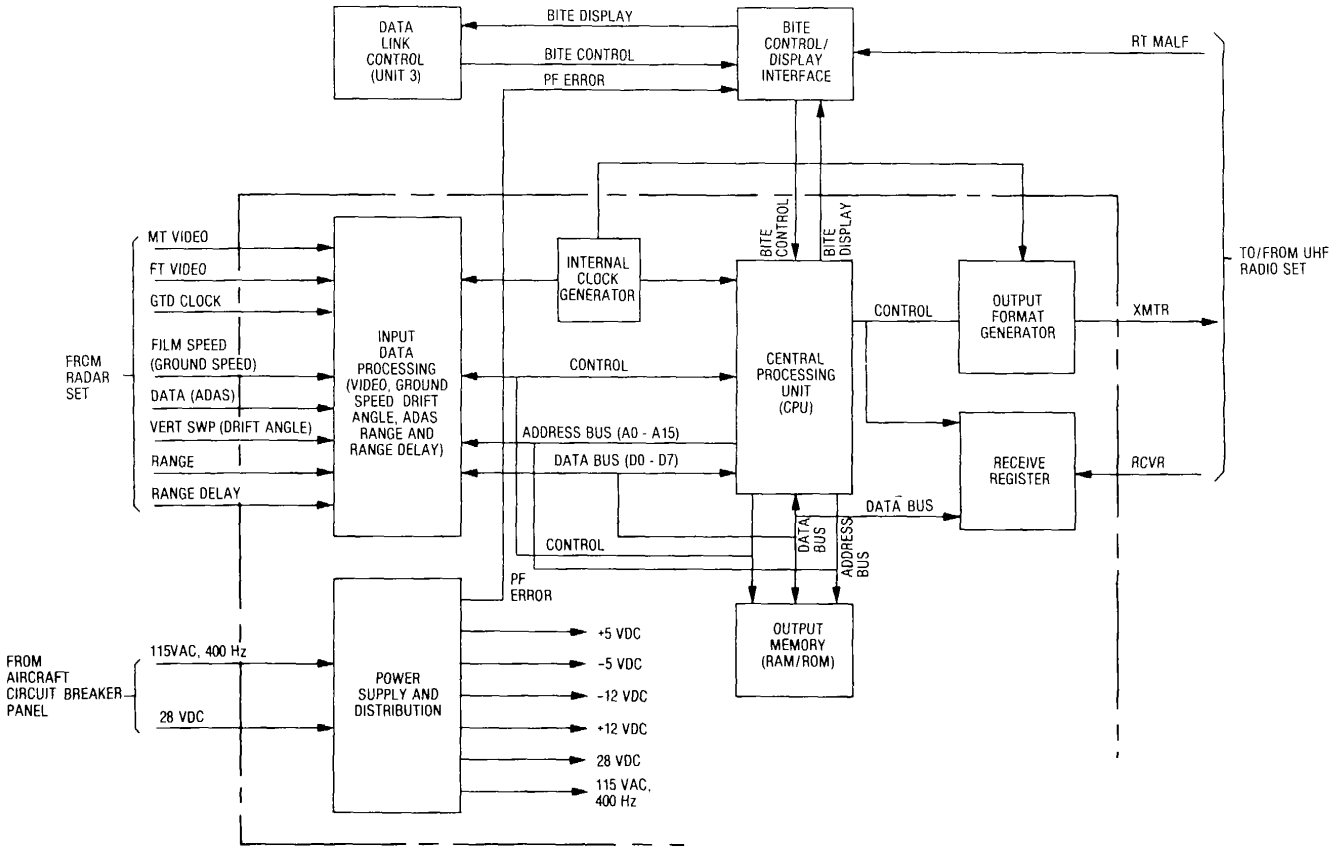


Figure 2-4. Encoding subsystem overall block diagram.

successive pulses The converted data, represented by two successive 8-bit data words (only 12 bits of which are used), is then transferred (via the data bus) to output RAM under CPU control

e. *Drift Angle Input Data Processing* Substitute aircraft drift angle input data (VERT SWP) is received in the form of an analog signal The slope of the VERT SWP signal varies in direct proportion to the vertical sweep signal in the radar recorder This permits drift angles to be measured regardless of the selected aircraft navigation mode (inertial or manual) Similar to the video data processing, analog-to digital conversion is performed prior to data transfer to the output RAM.

f. *Central Processing Unit* Data processing operations, with the exception of video input data processing, are under CPU/program control The respective programs are permanently stored m the read-only memory (ROM) portion of the output memory section. The program Instructions are executed by the CPU microprocessor, which transfers data via 8 parallel data lines and accesses memory locations via 16 parallel address lines CPU timing and synchronization are provided by a clock derived from the internal clock generator During the output transmit cycle, the CPU transfers data from the output memory to the output format generator where final data formatting is performed prior to downlink transmission During operator initiated BITE, control signals are received from the data link control, via the BITE control/display interface, for selection of the airborne and downlink BITE modes of operation BITE display signals are outputted to the data link control for BITE in-process and failure display.

g. Output Memory The output memory section consists of random access memory (RAM), read only memory (ROM), and associated interface and control circuits The RAM is used for storage of the variable data transmitted each frame to the ground station The ROM is used for storage of the fixed program code, which defines the repetitive operational sequences related to the processing, transfer, and formatting of data The interface circuitry consists of bidirectional networks used for transfer of data to/from memory, depending on the control logic status Should encoder power supply failure occur at any time during normal operation, encoder fault indication is provided. In this case error display is enabled by activation of the power fault error (PF ERROR) line Should uhf receiver-transmitter synchronization or low rf power failure occur at any time during normal operation, uhf receiver-transmitter fault indication is provided. In this case, error display is enabled through activation of the uhf receiver-transmitter malfunction (RT MALF)
line outputted by the uhf receiver-transmitter

h. *Output Format Generator* The output format generator organizes the data to be transmitted into a serial bit stream through operation of various registers and associated counting and control logic The data is processed in two word groups in accordance with the main output program instructions In the case of preamble data, no modification or addition to the data word bit structure is required, while mode and ADAS words require addition of three parity bits, resulting in a final format of 11 bits The video data is also modified from 8-bit to 11-bit format, however, the additional bits are obtained by simple redundant connections at the inputs of the respective registers

i. *Receive Register* The purpose of the receive register is to provide initial processing for the RCVR data outputted by the receiver section of the uhf receiver transmitter This processing operation, part of the online BITE provided by the encoder, is performed whenever data is being transmitted to the ground station. Upon accumulation of 11 data bits (one data word), the receive register data is clocked onto the data bus for transfer to the CPU section where it is checked for proper synchronization The period during which the data words are checked begins at ADAS and concludes at the start of video Should improper data synchronization be detected, a uhf receiver-transmitter fault indication is registered on the data link control

j. Power Distribution and Control The encoder receives 115 V ac, 400 Hz single-phase and 28 V dc primary power from the aircraft The 115 V ac is used primarily for generation of regulated ± 12 V dc and ± 5 V dc transistor supply voltages The 28 V dc is used for relay control and data link control indicator power. Power supply operational status is continuously monitored by power fault detection circuitry. Should any voltage exceed or drop below normal limits, power fault error (PF ERROR) is applied to the data link control, to illuminate the ENCODER FAULT indicator

k. Data Link *Control* In addition to providing BITE control/display facilties, the data link control provides selection of off, standby, and transmit modes of operation With respective selector switch set to off, all system functions cease In the standby mode of operation, the system is energized, with the exception of the transmitter section in the uhf receiver-transmitter BITE testing during standby operation is limited to the encoder In the transmit mode of operation, the system is fully operational BITE testing in the transmit mode encompasses both the encoder and uhf receiver-transmitter.

2-6. Encoder Programs

The majority of data processing, transfer, and formatting is done by four programs main-output, hardware interrupt, housekeeping, and BITE

*a. Main Output/Hardware Interrupt Programs The /*main-output program uses CPU interrupt circuitry to

synchronize data transfer from output memory to the output format generator for realtime serial downlink transmission During execution of the output program, data are transmitted in two-word groups Preamble/mode, ADAS, video A-field, and video B/C-field data are sent, respectively Following each two-word transmission, branching is performed to the hardware interrupt program, at which time further sequencing is dependent on interrupt status If presence of a transmit register interrupt is detected, the next two words in sequence are read from output memory for output formatting and transmission This cycle is repeated until transmission of data is complete If a transmit register interrupt is not detected at the start of the hardware interrupt program, a check for presence of ADAS input data is performed If present, the ADAS data is processed into memory Following execution of the ADAS sequences, drift angle data processing sequences are executed If a self-test (BITE) is in process during hardware interrupt program execution, program sequencing is modified to enable monitoring of test data and display of test results Selection of self test and display of test status is provided by the data link control unit Return to the main output program is accomplished at the end of the hardware interrupt sequence At the end of the main output program, an alternating 1/0 bit pattern is transmitted until the start of the next main output cycle

b. Housekeeping/Coldstart Programs Parameters which are updated during housekeeping include antenna mode, film speed, range/range delay, BITE request detection, ADAS input status, video B/C field select, and drift angle acquisition The housekeeping program is executed primarily during the time between the end of the video data output transmission and transfer of processed video data to output memory Near the end of the housekeeping sequence, the program waits for the transfer of video data before resumption of program sequencing Upon completion of the housekeeping sequence, branching is performed back to the main output program, at which time a new output cycle Is started An additional program, coldstart, is provided for initializing various program and hardware controls following a microprocessor unit (MPU) reset at equipment power-up

2-7. Internal Clock Generator Section

fig 2-5)

a. General The internal clock generator provides a series of reference frequencies derived as submultiples of a 20 MHz crystal-controlled reference oscillator The circuitry Is located on MPU/tlming module 2A11 Figure 2-5 provides block diagram details

b. Functional Description A 625 kHz signal is supplied to the output format generator and receive register section (para 2-15) for data word counting and 31 25 kHz is supplied to the ADAS data processing section (para 2-9) for ADAS clock simulation during BITE operation The video data processing section (para 2-8) receives 5 MHz, 2 5 MHz and 1 25 MHz signals, which are utilized during video data transfer operations, a B GTD 5 MHz signal, which is used during BITE operation in place of the externally derived video accumulation clock (GTD CLK), and a 6 Hz signal (L/R), which is used during BITE operation for simulated antenna switching The ground speed data processing section (para 2-10) receives a 125 kHz signal, which serves as a time base for unit counting, and an 83 Hz signal, which is used during BITE operation in place of the normal ground speed data signal

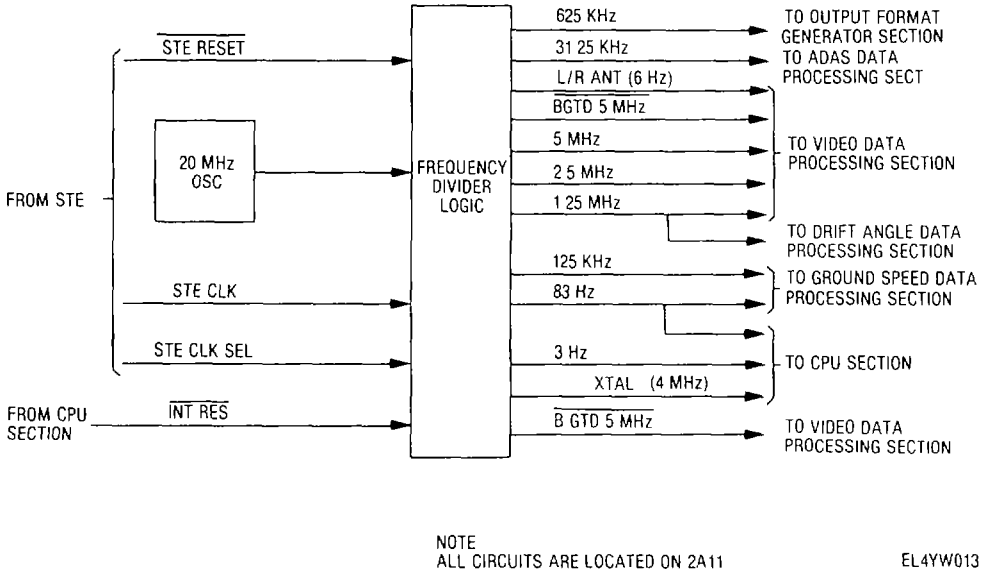


Figure 2-5. Internal clock generator functional block diagram.

(FILM SPEED) The CPU section (para 2-13) receives 4 MHz (XTAL), which serves as the microprocessor clock, and 3 Hz and 83 Hz signals, which are used for purposes of MPU lockup and power-on-reset generation During special test equipment (STE) operations, the 20 MHz internal oscillator signal is replaced by a 5 MHz STE clock signal (STE CLK) Selection between the internal 20 MHz signal and the STE CLK signal is provided by the STE CLK SEL signal Periodic resetting of the frequency divider logic during STE operation is enabled by the STE RESET signal During BITE operation, signal INT RESET transitions low to initialize the B GTD 5 MHz signal

2-8. Video Input Data Processing Section

(fig. FO-2)

a. General The function of the video data processing circuitry is to convert the FT and MT video inputs to digital form for serial transmission downlink. Two basic operations are associated with video data processing, data accumulation and data transfer. During data accumulation, the video data undergoes amplitude averaging over a fixed number of radar pulse repetition intervals (PRI) for each of 1680 range cells The range cells are grouped into three equal fields of 560 each, designated A, B and C, A-field being closest to the aircraft The averaging period for A-field is 256 PRI, while B/C-field averaging is performed over 512 PRI (Averaging over twice the A- field rate is possible due to widening of the radar beam width as the range from the antenna increases) Input data, during data accumulation, is sampled at a 5 MHz rate, using a gated 5 MHz clock signal supplied by the external equipment Since the upper frequency limitation of the accumulator memory is less than 5 MHz, accumulation is performed by two separate networks, each operating at a 2 5 MHz rate Essentially, data from all odd numbered range cells is accumulated by one network, while the other is used for accumulation of data from all even numbered range cells When accumulation is complete, average values are computed for each range cell Before transfer to the output memory section, special processing Is also performed whereby weaker targets receive enhancement by selective bit allocation During the data transfer period, the accumulated data for each range cell is transferred to the output memory section (via control of the video control board) for storage prior to downlink transmission A 1 25 MHz clock rate is utilized during data transfer operations The 1 25 MHz clock is generated internally and is asynchronous to the externally derived gated 5 MHz clock signal The video data processing circuits are located on video interface module 2A17, analog-to-digital (A/D) converter module 2A2, video control module 2A7, FT accumulator memories 2A3 (odd) and 2A4 (even), MT accumulator memories 2A5 (odd) and 2A6 (even), and video multiplexer module 2A9 b Input Amplification and Conditioning The MT and FT video input signals initially undergo amplification and conditioning on video interface module 2A17. Additional amplification on module 2A17 provides conditioning of the 5 MHz GTD CLOCK and ANTEN-NA GATE input signals The amplified MT and FT video signals, which are adjusted for a maximum level of +4 5V, are applied to respective analog-to-digital converters located on A/D converter module 2A2 The conditioned 5 MHz GTD CLOCK and ANT SELECT signals are applied as inputs to the video timing and control logic on video control module 2A7

c. Analog-To-Digital (A/D) Conversion The MT A/D converter samples the input video signal at a 200 ns (5 MHz) rate, providing a 3-bit output data word representative of video magnitude Since the required sample rate of 5 MHz exceeds the upper frequency limit of the temporary (accumulator) memory to be used for storage of the A/D data, a dual data processing network is used Essentially data from all odd range cells is processed by one network, while a similar network processes data from all even numbered range cells By dividing the data processing function in this manner, the individual network processing rate is reduced to 2 5 MHz, which is within the operating range of the accumulator memory elements Operation of the FTA/D converter is similar to the MTA/D converter except that FT magnitude resolution is expressed in the form of a 5-bit data word for each A/D sample Expressed as a function of voltage, MT threshold resolution is approximately 0 57V (7 X 0 57V - 4V), while FT threshold resolution is approximately 0 129V (31 X 0 129V - 4V)

d. *Video Accumulator Memories* Following A/D conversion the FT data is applied directly to corresponding odd and even accumulator memories (located on modules 2A3 and 2A4), while the MT data is routed to odd and even MT accumulator memories (located on modules 2A5 and 2A6) via a magnitude comparator/selector network (located on video multiplexer module 2A9) During single antenna (left or right) operation, the odd and even MT data is switched directly through the magnitude comparator/selector During both antenna (left and right) operation, comparison of adjacent range cell data is performed The larger of the MT target data, whether odd or even, is then applied to modules 2A5 and 2A6 via both the odd and even MT data lines This feature Insures retention of the primary MT target since, during both antenna operation, left antenna data is stored exclusively in the even MT accumulator memory, while right antenna data is stored exclusively in the odd MT accumulator memory The accumulation period for A-field data is 256 PRI, while the B/C-field accumulation period is 512 PRI

The accumulated MT data magnitude is expressed in the form of a 12-bit data word, while FT data magnitude is expressed in the form of a 14-bit data word Operation of the MT and FT accumulator memories is similar with the exception of range cell address count- ing, which is performed on the MT accumulator memory boards for use on both MT and FT accumulators When data accumulation is complete, the contents of the accumulator memories are unloaded, address by address, for final processing before storage m the out- put memory.

e. *Output Data Processing/Selection* Final processing of the accumulated MT and FT data is accomplished by the output data processing/selection circuitry (located on video multiplexer module A9) During final processing, average values are computed for each odd and even range cell The data then undergoes further processing to enhance the weaker targets with- out increasing overall bandwidth usage Specific pro- gram selection is a function of operating mode and field status Mode decoding is accomplished by sensing the level on the BOTH ANT line, which is high during both antenna operation, and on the AB/C line, which transitions high during B and C field periods The resultant output data, whether MT or FT, is expressed In 8-bit format The MT data consists of three data bits, three error correcting (Hamming code) bits, and two identification (ID) bits FT data consists of five data bits, two ID bits, and one parity bit The data format is as follows:

D7	D6	D5	D4	D3	D2	D1	DO
FT=FT4	ID	FT3	FT2	FT1	FTO	ID	P
MT=MT2	ID	MT1	MTO	H2	H1	ID	HO

The selected output data (MT or FT) depends on the MT data magnitude When the MT data magnitude is greater than a fixed reference magnitude, indicating a true MT target, MT data is transferred to the output memory for downlink transmission When the MT data magnitude is less than the reference magnitude, FT data is selected for transfer to the output memory

f. Timing and Control Timing and control during data accumulation and transfer is enabled by circuitry located on video control module 2A7 During data accumulation, the A/D converters receive timing signals ADLO and ADLE for latching each data sample The MT and FT accumulator memories receive signals ADLO and ADLE for latching each data word out- putted by the A/D converters Summing over the averaging periods for each range cell is enabled by clock signals RAOO and RAOE, which are derived from the GTD 5 MHz CLOCK input, at one-half the input clock rate (2 5 MHz) Circuitry for counting the radar pulse repetition mtervals is enabled by the LOAD signal, while signals MT DAINLAR, FT DAINLAR and R CLEAR provide periodic resetting of the accumulator memory logic Antenna mode status is conveyed to the CPU via the ANT XTN DET line, which is set high every time antenna switching occurs Periodic resetting of the antenna transition detection logic on module 2A7 is enabled by the XTN DET RESET line, which is reset (low) after acknowledgment of antenna transition detection by the CPU Read/write control of the accumulator memory elements is enabled by signals R/W-O and R/W-E, which transition low for writing data mto accumulator memory and transition high for reading data out of accumulator memory during data transfer HALT transitions low to signify start of the video data transfer period, during which time the microprocessor in the CPU section is disabled Should ADAS input data be received during video data transfer, the ADAS DISABLE signal transitions low, at which time additional video data transfer ceases until the present ADAS input data is processed into memory Upon completion of ADAS in- put data processing, ADAS DISABLE returns to a high level and video data transfer resumes Avail- ability of the data bus for transfer of video data is determined by sensing the VID BA signal level, which transitions high when the data bus is available for video data transfer Signal IWC transitions low to indicate to the output memory that valid video data is warning to be loaded Generation of the IWC signal is enabled by the gating of the 1 25, 2 5, and 5 MHz internal clock signals During data transfer, master tim- ing is derived from the 1 25 MHz clock supplied by the internal clock generator Consequently, the contents of the accumulator memories are read out at one- fourth the accumulation rate, in conjunction with clock signals RAOO and RAOE The signal INT RES, from the CPU section, resets the timing and control circuits *g Video BITE* BITE operation commences follow- ing transition of the BITE lihne to a high level In the BITE mode of operation, time varying test signals (MT BITE VID and FT BITE VID) are substituted in place of the normal MT and FT VIDEO signals Test voltage generation is enabled by signals B- FT, B-MT, RA5E and RA6E During video accumulation, signals RA5E and RA6E cause certain range bins to integrate (synchronously) to predetermined fixed voltage levels Signals B-FT and B-MT appear as fixed or switching levels, depending on the BITE sequence m progress During airborne BITE, the signals are fixed at a high level Following completion of three video integration cycles, data checks are performed for selected A, B, and C field values, in conjunction with high and low limit reference levels stored in the output memory ROM During downlink BITE, signals B-FT and B-MT are varied for purposes of generating a predetermined image on the ground station recorder It should also be noted that during BITE operation, an internally generated gated 5 MHz reference clock (B-GTD 5 MHz) is

substituted m place of the normal (externally derived) gated 5 MHz clock

2-9. ADAS Input Data Processing Section

(fig 2-6)

a. General The function of the ADAS input data processing circuitry is to convert the ADAS data to 8 bit parallel format for transfer to the output memory section The circuitry is located on ADAS control module 2A16 and output buffer module 2A12 Selector operation is controlled by the DO output of the input data latch, which transitions low during normal operation, thereby selecting ADAS input data from the radar set Following selection of the airborne or downlink BITE test mode by the operator, DO transitions high, thereby selecting simulated ADAS data generated by the encoder BITE circuitry Clocking of the input data latch occurs on the negative transition of signals WC and 0002 From the data selector, the ADAS data bits are accumulated m a 12-bit shift register, while the MODE, CLOCK and R/W signals are routed to various counting and control circuitry During certain valid sample periods, the level of MODE indicates whether the next block of ADAS data will be m BCD or numeric form At all other times the MODE level has no meaning A low level during a valid sample period indicates the next block of ADAS data will be in BCD form, while a high level indicates numeric ADAS data In any case, whichever level is present on the MODE line is clocked onto the BCD MODE line when the ADAS CLOCK signal transitions high.

b. *Functional Description* Following initial amplification, the ADAS signals (DATA, CLOCK, MODE and R/W) are applied to a selector stage together with respective BITE equivalents The level on the BCD MODE line, in turn, is transferred to the data bus as D2 data Enabling of the respective bus driver takes place during low level coincidence of signals 2002 and RC Counting of the ADAS data bits (for determination of word length) commences upon positive transition of the R/W input signal (prior to such time the ADAS CLOCK pulse counting is inhibited) After loading one ADAS data word (8-bits) and four unused parity bits into the 12-bit serial register, the ADAS RDY line transitions high to notify the CPU section that ADAS data is ready for processing into memory In response to the ADAS ready interrupt, signal hnes 2004 and RC transition low to transfer the 8-bit ADAS

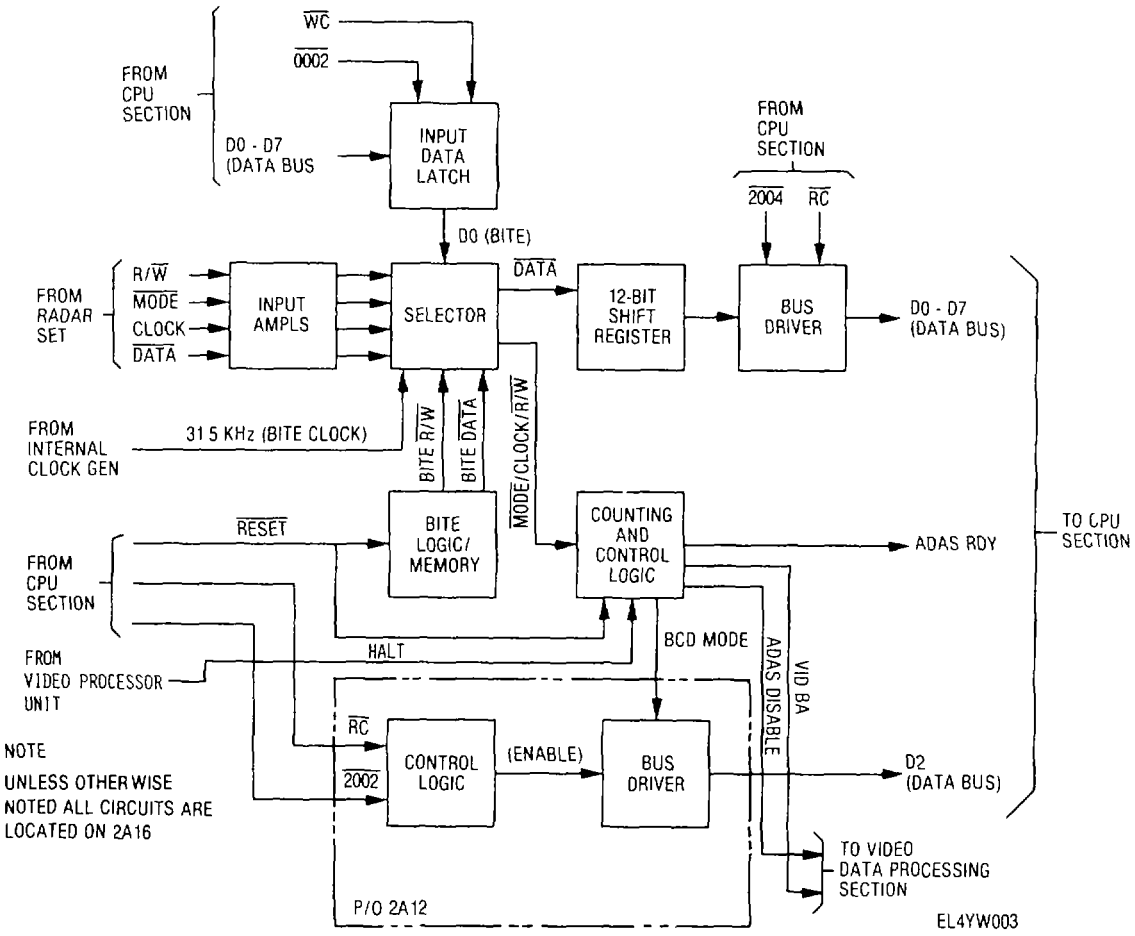


Figure 2-6. ADAS input data processing functional block diagram.

data word onto the data bus The cycle is repeated un-til a total of 48 ADAS words are processed The various counting and control logic is started by signal RE-SET Signals VID BA and ADAS DISABLE are de rived from the control logic for application to the video data processing section, where they are used to halt video data transfer during periods ADAS input data is simultaneously being received

c ADAS BITE During BITE operation, the DO out-put of the input data latch transitions high, causing simulated test data to be substituted m place of the normal system data Simulated ADAS data words are derived from BITE memory, while other BITE circuits provide the logic necessary for simulation of the ADAS R/W control signal ADAS clock simulation is provided by a 31 2 kHz BITE clock derived from the internal clock generator A + 5 volt level is substituted for the MODE signal to simulate BCD format

2-10. Ground Speed Input Data Processing Section (fig 2-7)

a. General The function of the ground speed input data processing circuitry is to convert ground speed input signals received from the radar set to 8-bit parallel format for transfer to the output memory section The circuitry, located on ADAS control module A16, consists functionally of an input ampflifier and data latch, data selector, gated counter and control logic, and bus drivers.

b. Functional Description Aircraft ground speed is obtained directly from a film speed sensing circuit located in the radar set recorder Film speed, in turn, is a function of ground speed, range, and antenna mode The input signal (FILM SPEED) is received in the form of a variable pulse rate stream The higher the ground speed the faster the pulse rate, the higher rate being 644 64 PPS at 300 knots/25 km/single antenna The lowest rate of 40 29 PPS at 100 knots/100 km/both antennas The measurement technique consists of counting a fixed rate clock between two successive FILM SPEED pulses Following initial amplification, FILM SPEED is applied to the data selector, along with an 83 Hz BITE reference signal Operation of the data selector is controlled by the DO output of the input data latch, which is clocked low during normal operation in conjunction with signals 0002 and WC While DO is low, the FILM SPEED signal is applied to the grated counter and control logic The gated counter is enabled under program control by data signal D5 When D5 goes high, the control logic is G1iabled and the counter is gated on by the next high-to-low transition of FILM SPEED The *counter* is gated off by the second high-to-low transition and a flag bit is generated When the flag bit is read by the CPU in conjunction with signals 2000 and RC, *ihe* counter's output is then read using signals 200B-EN and 200C-EN The counter output is two 8-bit words whose combined value corresponds to the number of 125 kHz cycles counted between the two consecutive

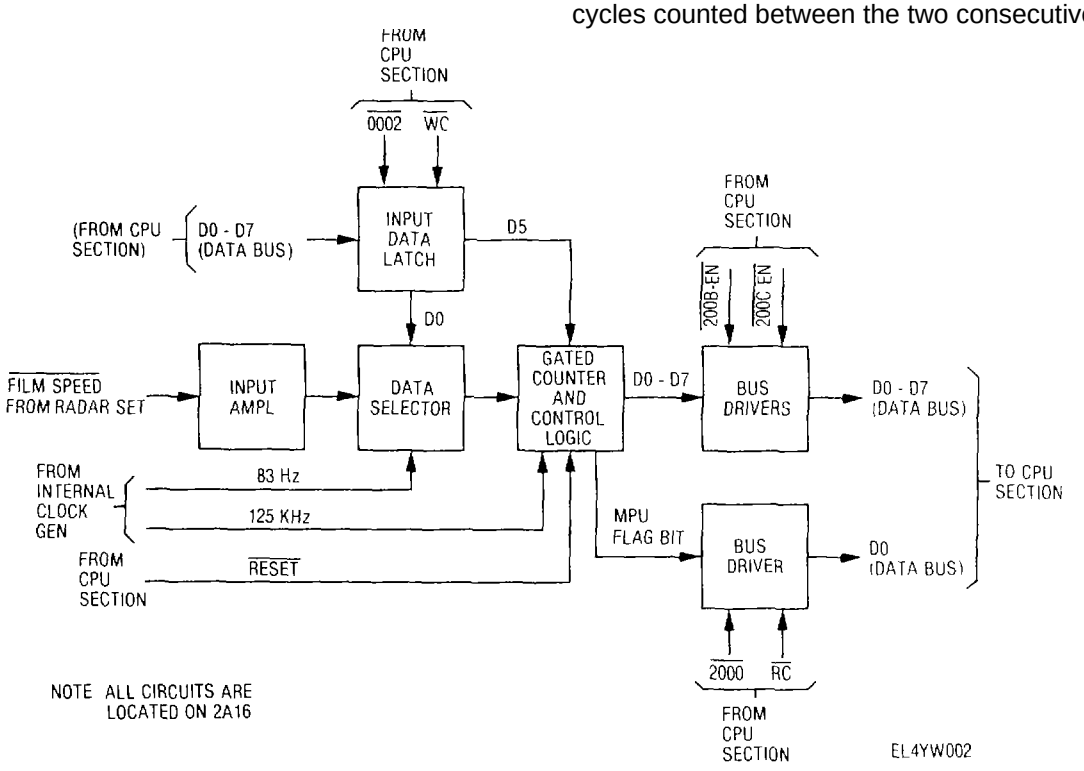


Figure 2-7. Ground speed data processing functional block diagram.

FILM SPEED falling edge transitions After the counter has been read, D5 goes low, which restarts the control logic and counter Then D5 returns high to enable the next ground speed sample cycle

c. Ground Speed BITE During BITE operation, high level DO data is applied to the data selector, thereby substituting a fixed rate test signal (83 Hz) in place of the FILM SPEED signal The resultant output data words are then checked by the CPU against high and low limit references stored m the output memory ROM Clocking of the DO and D5 data through the in-put data latch is enabled by signals 0002 and WC

2-11. Drift Angle Input Data Processing Section

(fig 2-8)

a General The function of the drift angle Input data processing circuitry is to convert drift angle input signals received from the recorder to 8-bit parallel format for transfer to the output memory section The circuitry is located on power fault detector module 2A13

b Functional Description Aircraft drift angle is computed by measuring the slope of the vertical sweep signal generated by the radar set Following buffering and input switch selection, the VERT SWP input signal is differentiated and then amplified The amplifIcation factor is controllable and depends upon range and antenna mode Control is accomplished in conjunction with operation of the Input data latch and analog switch Input signals AO, 0000 and WC are used for clocking-in data bits D1 and D2, which regulate the amplifier gain via the analog switch Maximum gain results when the data bits are high, while minimum gain occurs when both data bits are low In voltage terms, the amplifier output is scaled to provide a maximum swing of t V for a given input Following amplification, the vertical sweep signal undergoes analog to-digital conversion to the system 8-bit word format The A/D conversion rate of 64 microseconds is based on a clock frequency of 625 kHz The 625 kHz, in turn, is derived by dividing a 1 25 MHz input clock by two The A/D converter is enabled by signal ST ADC Following analog-to-digital conversion, the eight bits of

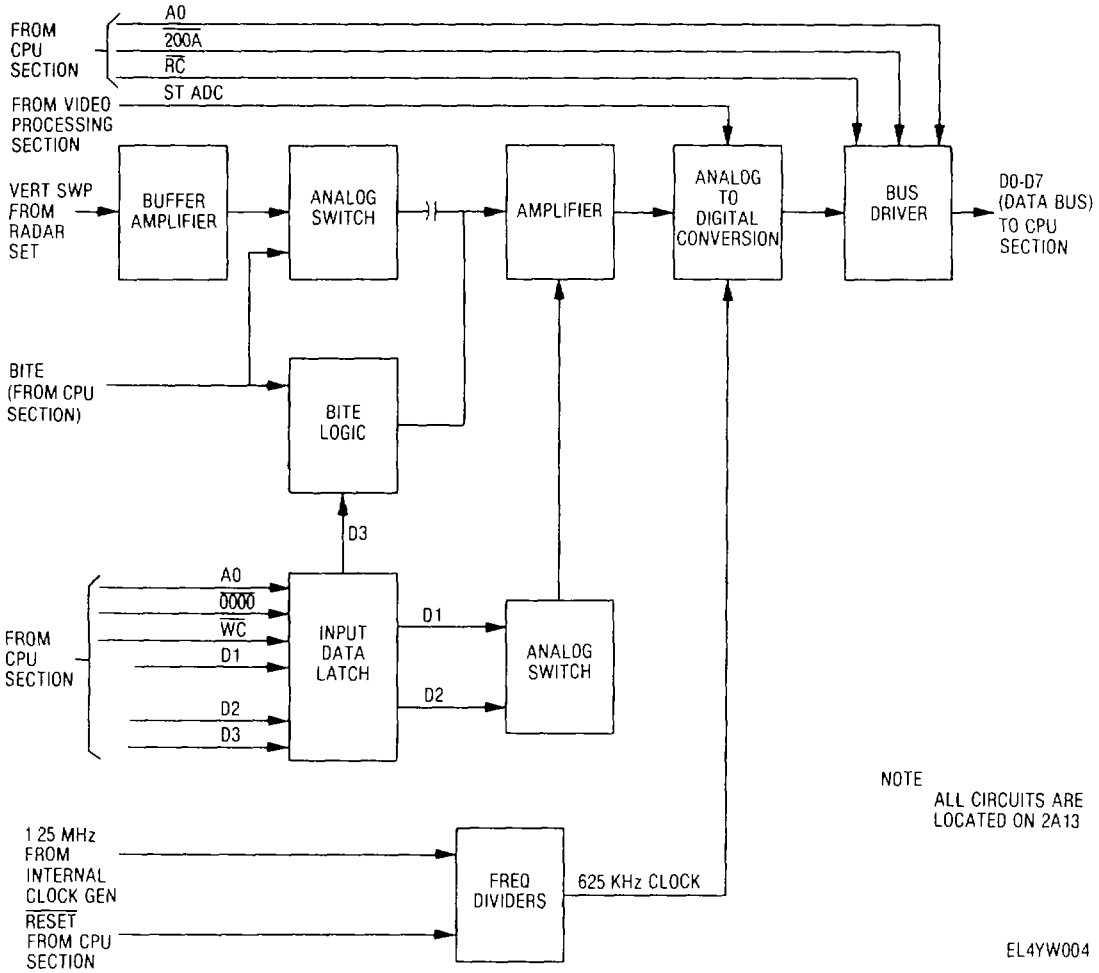


Figure 2-8. Drift angle input data processing functional block diagram.

data undergo transfer to the data bus via the output bus driver which is enabled by signals RC, 200A and AO The 1 25 MHz frequency divider is started by the RESET signal from the CPU section

c Drift Angle BITE During BITE operation simulated vertical sweep data is generated by the BITE logic BITE operation commences when the BITE in-put line transitions high, at which time the input analog switch is open-clrculted with respect to the VERT SWP signal At the same time, test signals are substituted in place of the VERT SWP signal Test signal magnitude is generated as a function of data bit D3 When D3 is low, a + 5V level IS applied to the amplifier stage, while a - 5V level is applied when D3 transitions high Circuit performance verification is based on comparison of the output data to reference data stored In output ROM for three gain/input level conditions

2-12. Range and Range Delay Input Data Processing Section

(fig 2-9)

a. General The function of the range and range delay input data processing circuitry is to convert the range and range delay signals received from the radar set signal processor to 8-bit parallel format for transfer to output memory The circuitry, which consists basically of data input buffers, a data bus driver, and associated control logic, is located on power fault detector module 2A13

b. *Functional Description Range* information is received on the RNG (25-50) lines Range selection is indicated by high level transition of the corresponding line A combination of both lines going low represents 100 km range Range delay information is received on the six DLY (0-50) lines, which go high (individually) to indicate respective range delay A combination of all range delay lines going low represents 60 km range delay Reading in of the range and range delay data is accomplished (under program control) using the gated resultant of CPU signals AO, 2008 and RC (read command) to enable the gated bus driver Output data signals DO through D5 represent range delay, while the combination of D6 and D7 represent range Once present on the data bus the range and range delay data undergoes processing by the CPU for storage in the output memory

2-13. Central Processing Unit(CPU) Section

(fig. FO-3)

a. General The function of the CPU is to execute the operational programs associated with transfer, storage, and outputting of the digitized radar data The various operational programs executed by the CPU are stored m permanent memories (ROM) located in the output memory section The circuitry comprising the central processing unit is located on MPU/timing module 2All, output buffer 2A12, power fault detector 2A13, and ADAS control 2A16 Figure FO-3 provides block diagrams

b. Microprocessor The primary functional element in the CPU is the microprocessor (MPU), which is abdirectional, bus-oriented 8-bit (DO-D7) parallel device, with 16 bit (AO-A15) address capability MPU operation is enabled in conjunction with the following timing and control functions:

XTAL.--This input serves as the basic unit clock for the microprocessor

HALT-When this input transitions low, the microprocessor is disabled to allow use of the data bus by the video data processing section for purposes of transferring MT and FT target data to the output memory

RESET-This output is generated by the power-on reset circuit for purposes of starting various functional circuits within the encoder BA-This output signal (normally low) transitions high to indicate that the microprocessor is disabled

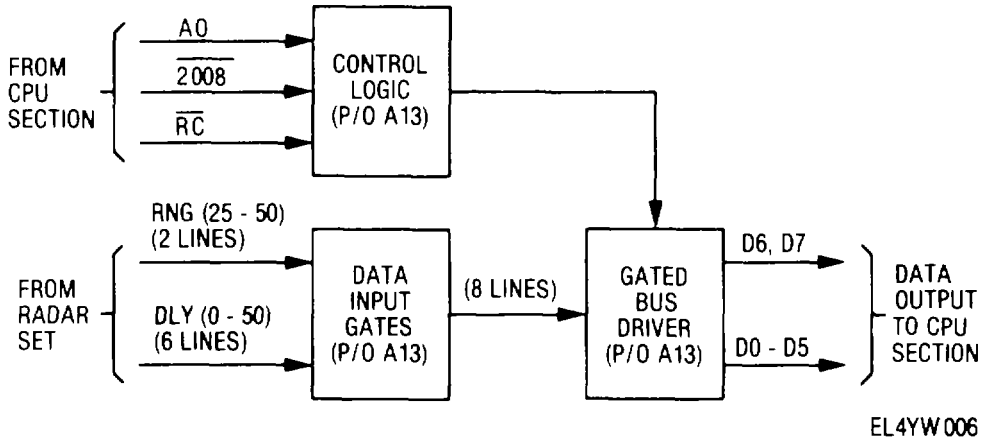


Figure 2-9. Range and range delay input data processing functional block diagram.

and the address data bus is available for general use VALID MEMORY ADDRESS (VMA)-Thls output signal indicates that a valid address is present on the address buq and Is used in conjunction with other signals (R/W and 02) to gate data and outputted by the microprocessor
READ/WRITE (RW)-This output signal indicates whether the microprocessor is in a read (high) or write (low) state.
Φ2-The falling edge of this internally generated microprocessor clock transfers data between the microprocessor and peripheral devices
OUTBUF IRQ (OUTPUT BUFFER INTERRUPT REQUEST)-This input requests that an interrupt sequence be started Start of the interrupt sequence is delayed until completion of the current instruction NMI (NONMASKABLE INTERRUPT)-This input signal (normally high) transitions low to request that a nonmaskable interrupt sequence be started by the microprocessor As with the OUTBUF IRQ signal, the microprocessor completes execution of the current instruction before recognizing the NMI signal

c. Data Bus Transceivers Transfer of data (DO-D7) to and from the microprocessor is accomplished through data bus transceivers Directional control of the data bus transceivers is dependent on the status of signals BA, VMA, R/W and Φ2, as monitored by the control logic When BA transitions high, a low enable level is applied to the data bus transceivers, thereby preventing MPU from the writing of data and making the data bus available for other sections The MPU address signals (AO through All and A15) to the output memory are applied through address bus drivers Control of the address bus drivers is dependent on the status of signal BA, as monitored by the control logic Enabling of the address bus drivers (via a low level) occurs while the BA line is low

d. *Interrupt Detection* Logic Interrupt sequence are initiated by the interrupt detection logic upon sensing an interrupt request in the form of a low level transition on any of four interrupt lines The four basic interrupts are ADAS RDY (ADAS data ready), CLEAR (drift angle data ready), RT DATA ERROR, and XMIT REG (transmit register empty) MPU notification of an interrupt request is enabled by high level transition of the OUTBUF IRQ line In response to the interrupt request, the MPU outputs hexadecimal address 2002 on the address bus, which is returned to the interrupt detection logic (via the hardware address decoding logic) in decoded form as signal 2002 At the MPU interrupt detection logic, signal 2002 is gated with Φ2 and RC, the resultant of which is used to clock interrupt source data onto the data bus for readout by the MPU The specific data bits used for identification of the interrupt sources are D3 (RT DATA ERROR), D4 (CLEAR DRIFT ANGLE), D6 (ADAS RDY) and D7 (XMIT REG) Once interrupt identification is made, the MPU proceeds to generate an address corresponding to the particular function as follows 200A (drift angle), 2004 (ADAS), 2008 (receive register), 0006 and 0007 (transmit register) In the case of drift angle, ADAS and receive register, the address functions are used to gate formatted data onto the data bus for storage in the output memory The transmit register address functions (0006 and 0007) are used to control transfer of data from the data bus to the output format generator The receive register, furthermore, is addressed only during a BITE sequence and only in conjunction with a transmit register interrupt If at any time a second interrupt is received while an existing interrupt sequence is in progress the second interrupt is stored for the remainder of the existing sequence, and then processed accordingly

e. *Gated Bus* Driver Logic During normal operation, the microprocessor is periodically updated, with various status and operational data, using gated bus driver logic for interface purposes The information is inputted to the microprocessor via the data bus Antenna transition detect status, B/C field select status and video data transfer (HALT) status are derived from the video data processing section and inputted to the microprocessor in the D7, D6 and DI bit positions, respectively Receiver-transmitter operational status is derived from the uhf receiver-transmitter and inputted to the microprocessor in the D5 bit position, a one representing a detected sync or power malfunction Encoder transmit/standby status is derived from the data link control and inputted to the microprocessor in the D2 position, a one represents standby and a zero represents transmit mode BITE request status is also derived from the data link control, with signal latching performed prior to application to gated bus driver logic Separate downlink BITE and airborne BITE requests are generated, airborne BITE request is inputted to the microprocessor in the D3 bit position, while downlink BITE request is inputted in the D4 bit position Gated bus driver is enabled by signals 2000 and RC Left/right antenna status is received from the video data processing section by a second gated bus driver network and inputted to the microprocessor in the D1 position In this case, a one (high) represents right antenna and a zero (low) represents left antenna This gated bus driver is enabled by signals 2002 and RC

f. *Synchronous Control Signal Logic* In addition to receiving status information in the form of synchronous data, the microprocessor outputs synchronous control signals Interface between the data bus and user circuits is accomplished through a series of binary latches Signals for controlling the encoder BITE IN PROCESS indicator (EN BIPL) on the data line control and resetting the video data processing cir-

cuitry (INT RES) and BITE request latches (BTR RES) are generated as a function of data bits DO, D4 and D5, respectively Latch clocking is enabled by signals 0000, WC and AO To activate the BITE IN PROCESS indicator, the EN BIPL line is set high, resulting in lamp conduction via the BITE LITE line Resetting of the video data processing circuitry and BITE request latches is enabled by setting the INT RES and BTR RES lines low Signals for controlling the ENCODER and R/T FAULT indicators (on the data link control), and for multiplexing associated with selection of BITE references sources (BITE, B-FT, B-MT), are generated as a function of data bits DO, D6 and D7, respectively Latch clocking is enabled by signals RC and 0002 Illumination of the ENCODER and R/T FAULT indicators (as a result of BITE, power supply or R/T sync failure) is enabled similar to illumination of the BITE IN PROCESS indicator, with respective lamp drive provided via the ENCDR ERROR and R/T LITE lines Setting the BITE line high results in substitution of BITE data in place of normal system data Simulated FT and MT video signals are introduced by setting the B-FT and B-MT lines high Signals for defining unit under test (TEST ENC), for resetting the antenna transition detection circuit, and for definition of the both antenna mode of operation (BOTH ANT) are generated as functions of data bits D3, D5 and D4, respectively Latch clocking is enabled by signals RC and 0004 Setting the TEST ENC line high results in test data monitoring at the output of the encoder, while a low level results in test data monitoring at the output of the encoder, while a low level results in test data monitoring at the output of the uhf radio set Setting the RESET XTN DET line high starts the antenna transition detector in the video data processing section Following four successive detected antenna transitions, the BOTH ANT line is set high to provide notification to the video data processing section of recognition of the both antenna mode of operation

g. Error Source Signals Error source definition signals are provided to aid in performing troubleshooting when BITE performance results in a fault indication The error source signals consist of OUTPUTIRECV IRF, for an output or receive register fault, ADAS IRF, for an ADAS data processing fault, VID "A", for a A-field video fault, VID "B", for a B-field video fault, VID "C" for a C-field video fault, FILM SPD, for a film speed data processing fault, DRIFT ANG, for a drift angle data processing fault, and R/T (DATA), for an R/T data fault The error source signals are generated as functions of data bits DO-D7, respectively Latch clocking in this case is enabled by signals WC and 0000

h. Hardware Addressing In addition to being used within the CPU section, a variety of control and address functions are distributed throughout the encoder in support of related data processing operations Signals OXXX, BA, WC, All, A15 and $2 are applied to the output memory section, while the output format generator and receive register section receives signals RC, WC, 0006, 0007, 2006 and 2008 Drift angle input data processing is enabled by signals RC, WC, AO, 0000 and 200A, while signals RC, 2008 and AO are utilized for range and range delay input data processing Signals utilized for ADAS input data processing include WC, RC, 0002, 2002 and 2004, while synchronous gating of ground speed input data is provided by signals 200B-EN and 200C-EN, which are generated from signals RC, AO, 200A and 200C

i. MPU Reset The master reset line (RESET) is driven low following power turn-on and when the microprocessor falls to recycle within normal time lim-its (MPU lock-up) The power-on reset time lasts approximately 28 milliseconds (ms) and is a function of frequency counting and R-C delay time An 83 Hz signal serves as the basis for frequency counting If MPU lock-up occurs, as evidenced by absence of transitions on the OUTBUF IRQ line, a timeout sequence is initlated, utilizing the 3 Hz signal After eight cycles (2 6 sec) have elapsed, the RESET line is automatically driven low to reset the encoder circuitry

2-14. Output Memory Section

(fig 2-10)

a. General The function of the output memory is to provide temporary storage of the variable radar data periodically transmitted downlink and permanent storage of the preamble and MPU program code The radar data transmitted within each frame consists of one mode word, 48 ADAS words and 1120 video words The variable data is stored in random access memory (RAM), while all fixed data is stored in read only memory (ROM) The output memory circuitry is located on output memory module 2A14 Figure 2-10 provides block diagram details

b. *Data Bus Transceivers* Two-way interface with the system data bus is provided by the data bus transceivers Directional control of the data bus transcelvers is provided by the control logic in accordance with control signals RC (read control), OXXX and BA (bus available) Transfer of data into memory occurs when the RC line transitions high, at which time I/O SELECT input to the data bus transceivers transitions low Transfer of data onto the data bus occurs when RC, OXXX and BA transition low, at which time I1O SELECT transitions high

c. Data Reading/Writing Two configurations exist for writing data into memory One configuration is used for writing the video data outputted by the video processing section The other configuration is used for writing into memory the remaining variable radar

data to be transmitted downlink with the video data During the video write mode, video accumulator address signals RAO through RA10 are selected for application to the RAM For writing the remaining variable data into memory, addressing Is performed under MPU control using MPU address lines AO through A10 For purposes of address selector control, signal BA transitions high during the video write mode and low for MPU controlled writing

d. Read/Write Control Read/write control of the RAM is accomplished by signals IWC (integrator write control) and WC, which transition low during respective write periods IWC is used for video writing, while WC is used for MPU controlled writing Control of the RAM is enabled by signals Φ2, BA, and OXXX from the CPU section and M10 from the bus driver For reading data out of RAM, low or high M10 and low OXXX or BA combine to produce a low level on the RAM enable line Inhibiting of the RAM outputs, as represented by a high level on the enable line, occurs during the period signal Φ2 is high and BA is low This allows other sources to output data onto the data bus free of RAM interference Reading MPU program code out of ROM is enabled (under CPU control) by input signals BA, RC, A15, All and locally derived signal M10 Addressing is provided by input signals AO through A10 During ROM operations, directional control of the data bus transceiver is accomplished as previously described for RAM operation, except signals BA, A15, A11 and M10 (in combination) perform the function of signal OXXX These same signals are also used for generation of the ROM enable, which goes low to allow access to the ROM contents by the data bus transceivers

2-15. Output Format Generator and Receive Register Sections

(fig 2-11)

a. Output Format Generator

(1) *General* The function of the output format generator is to process preamble, mode, ADAS, and video data into final format for transmission downlink During the final processing, sequence data is serially outputted in groups of two 8-bit parallel words, under CPU control Following transmission of each two-word data group, an interrupt request (XMIT REG) is generated, at which time the next two 8-bit words In sequence are fetched by the CPU micro-processor and placed on the data bus for final processing The sequence is repeated untill all data words have been transmitted The output format generator circuitry is located on output buffer module 2A12 Figure 2-11 provides block diagram details

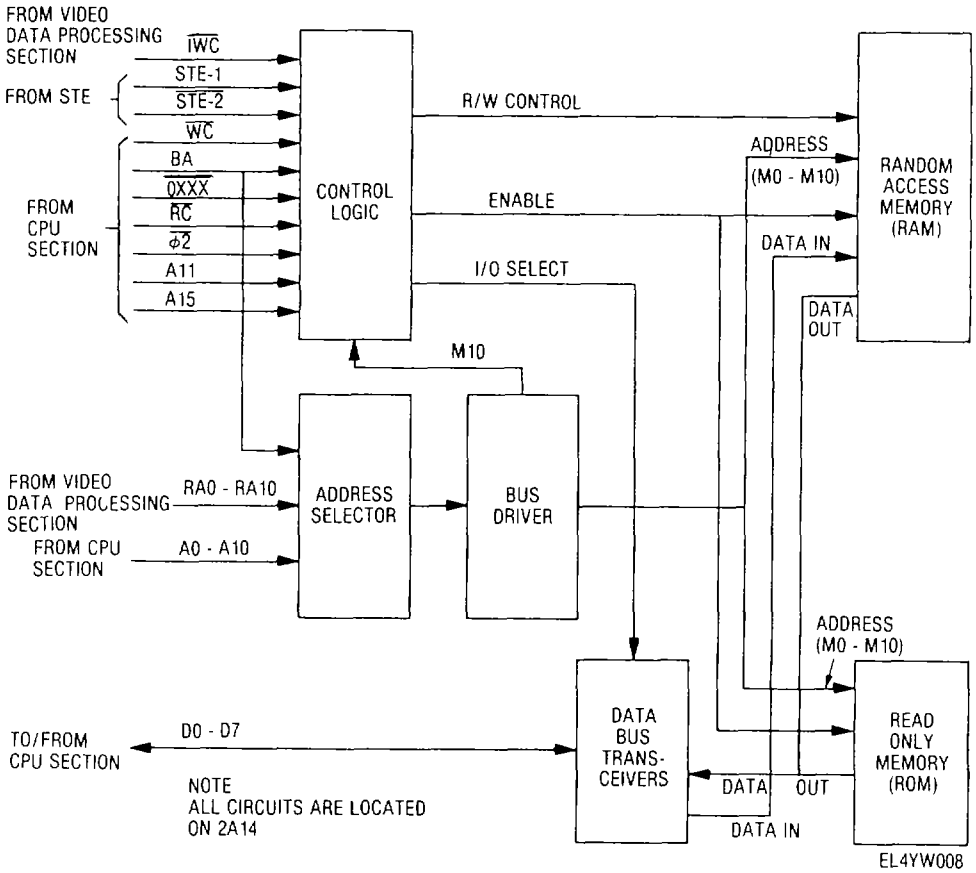


Figure 2-10. Output memory functional block diagram.

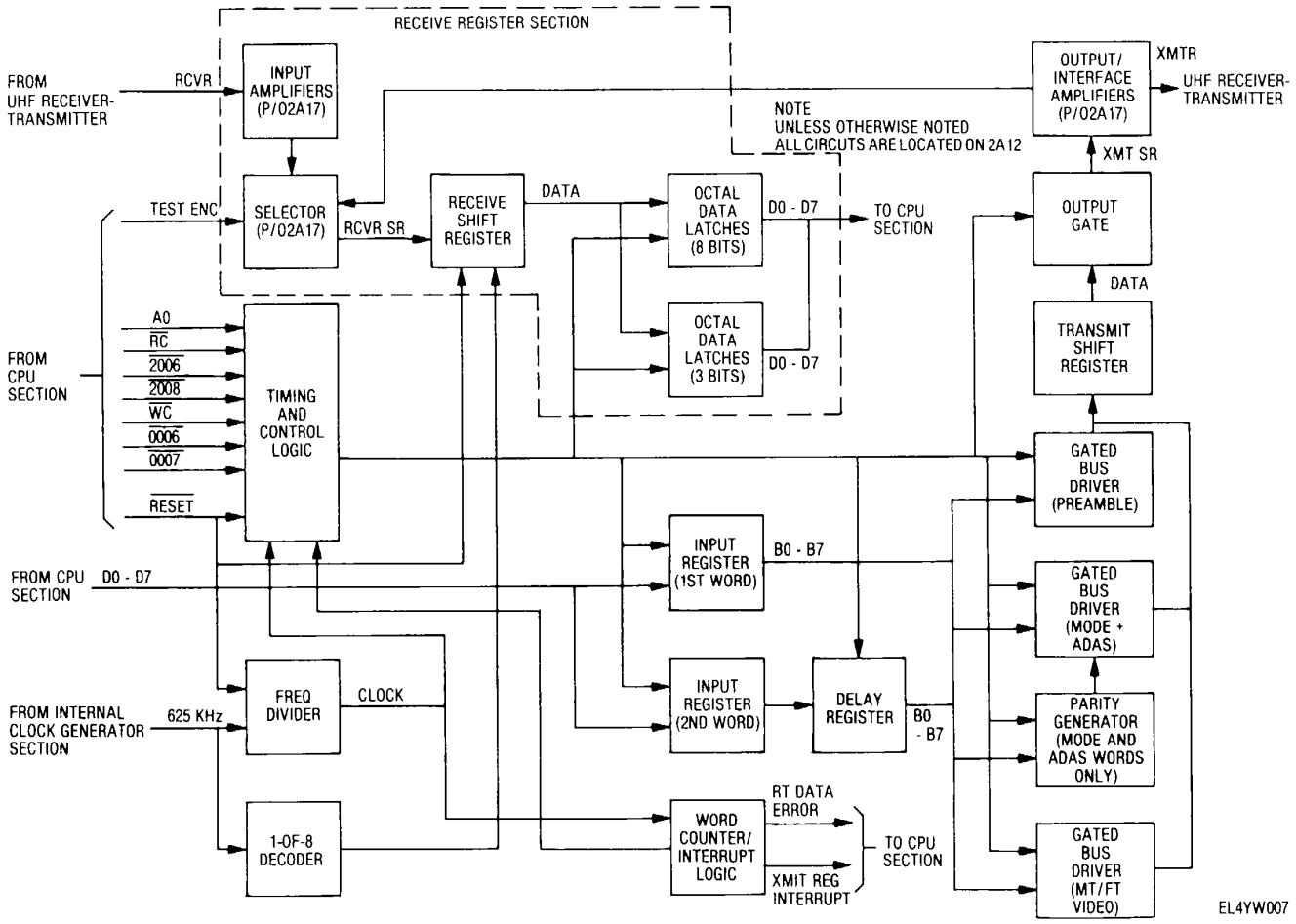


Figure 2-11. Output format generator and receive register block diagram

(2) *Input register logic* The data to be transmitted is initially loaded into the first and second word input registers First word register clocking is enabled by the timing and control logic input signals WC and 0006 Signals WC and 0007 are used to generate the clock for the second-word register The outputs of the input shift registers are applied to gated bus drivers for sequence formatting Prior to application to the gated bus drivers, the output of the second word register is applied to a delay register This permits double-word input processing without interferring with the loading of formatted words into the output shift register Word length for purposes of processing the various data is determined by dividing a 625 kHz input clock by 15, and using the resultant 41 667 kHz to cycle a word counter/interrupt logic network The timing and control circuitry is started by the RESET signal

(3) *Preamble formatting* Preamble words are the first words transmitted and require no modification to their bit structure During preamble, the word counter logic is preset to a count of eight When a count of 15 is reached, a signal is applied to the timing and control logic, in preparation for loading of the transmit shift register, which occurs on the next (16^{th}) clock cycle During the 16^{th} clock cycle, the first word input register (being previously enabled) is parallel loaded into the output shift register (via the preamble gated bus driver) At the same time, the delay register is enabled, so that on the next word count the data from the second word input register is parallel loaded into the output shift register During the second word count, the first word data is serially outputted by the output shift register Upon output shifting of the word from the second word register, an XMIT REG interrupt is generated, at which time the next two preamble words are loaded into the output format generator As a final processing step, the serial output data is applied through an output gate which performs polarity inversion on alternate words for purposes of polarity equalization

(4) *Radar mode and ADAS formatting* Following transmission of preamble data, radar mode and ADAS data are generated Processing in these cases, how-ever, is modified by the addition of three parity bits to each 8-bit word, and presetting of the clock counter to a count of five The parity scheme involves generating an odd parity bit for the high and low order four bits of each data word, and then generating a third parity bit based on the status of the high and low order parity bits With the inclusion of parity bits, the mode and ADAS data, in final form comprising 11-bit words, is parallel loaded into the output shift register and serially transmitted in a manner similar to the preamble data Again, processing is performed in two word groups, while alternate word polarity inversion is provided by the output gate .

(5) *MT and FT video formatting* Following transmission of mode and ADAS data, the MT and FT video data is transmitted Although the MT and FT word meanings are significantly different, the system out-put formatting is accomplished using the same logic circuitry In either case (MT or FT), the 8-bit input for-mat is converted to the appropriate 11-bit output for-mat by simple redundant connections at the MT/FT gated bus driver Again, processing is performed in two word groups and alternate word polarity Inversion is provided by the output gate

b. Receive Register

(1) *General* The function of the receive register is to process encoder and uhf receiver-transmitter output data during BITE operation The circuitry is located on video Interface module 2A17 and output buffer mod-ule2A12(fig 2-11)

(2) *Functional description* During the first phase of BITE operation, the data output of the encoder is serially loaded into the receive shift register through selector circuitry Selector control, in turn, is enabled by the TEST ENC signal, which transitions high during the period the encoder output is to be sampled When TEST ENC transitions low, the output of the uhf receiver-transmitter is selected for application to the receive shift register Prior to application to the receive register, the uhf receiver-transmitter output undergoes amplification The receiver shift register is clocked using a submultiple of the 625 kHz signal received from the internal clock generator section, with frequency division being performed by a 1-of-8 decoder circuit After a complete data word (11 bits) is loaded into the shift register, the data is sequentially transferred to the data bus, in 8-bit increments, for processing by the CPU The data transfer is accomplished by respective tristate octal data latches As a first step, simultaneous clocking of the first and second word latches is enabled by operation of the timing and control logic The respective clock inputs are de-rived from the word counter and frequency divider logic Once the data is latched, sequential gating of each octal data latch occurs, at which time the data is transferred to the data bus The first 8-bit word to be transferred contains the low order bits and is clocked out in conjunction with signals $\overline{2006}$ and $\overline{RC}$ The second word, which contains the high order bits, is clocked by signals 2008 and RC The receive shift register is initialized on the negative transition of $\overline{RESET}$

2-16. Power Supply and Distribution Functional Description

(fig 2-12)

Primary power consisting of 115 V ac, 400 Hz (single phase) and +28 V enters the encoder and is applied to EMI filter FLI From Fll, the +28 V is applied to

power relay K1 and to power fault detection logic located on power fault detector module 2A13 In addition, +28 V is supplied to the data link control for lamp power From FL1, the 115 V ac is applied to contacts of relay K1 Relay K1 is energized by placing the power switch on the data link control in the STBY or XMT position, at which time the CONT PWR line goes low With relay K1 energized, 115 V ac is then applied to +5 volt power supply PS1, -5 volt power supply PS2, ± 12 volt power supply PS3, blower B1, and elapsed time meter M1 The power supplies furnish regulated operating voltages for the encoder circuitry, and feature current limiting for overload protection An externally accessible potentiometer on each power supply permits nominal output voltage setting For encoder protection, overvoltage sensors are located across each power supply output Power supply functional status is monitored continuously In conjunction with operation of the power fault detection logic and ENCODER FAULT indicator on the data link control As long as the power supply voltages remain normal, the PF ERROR line is grounded causing the ENCODER FAULT indicator to remain off Should any power supply voltage drop below or rise above normal, the PF ERROR line is sent high by the power fault detection logic, illuminating the ENCODER FAULT indicator

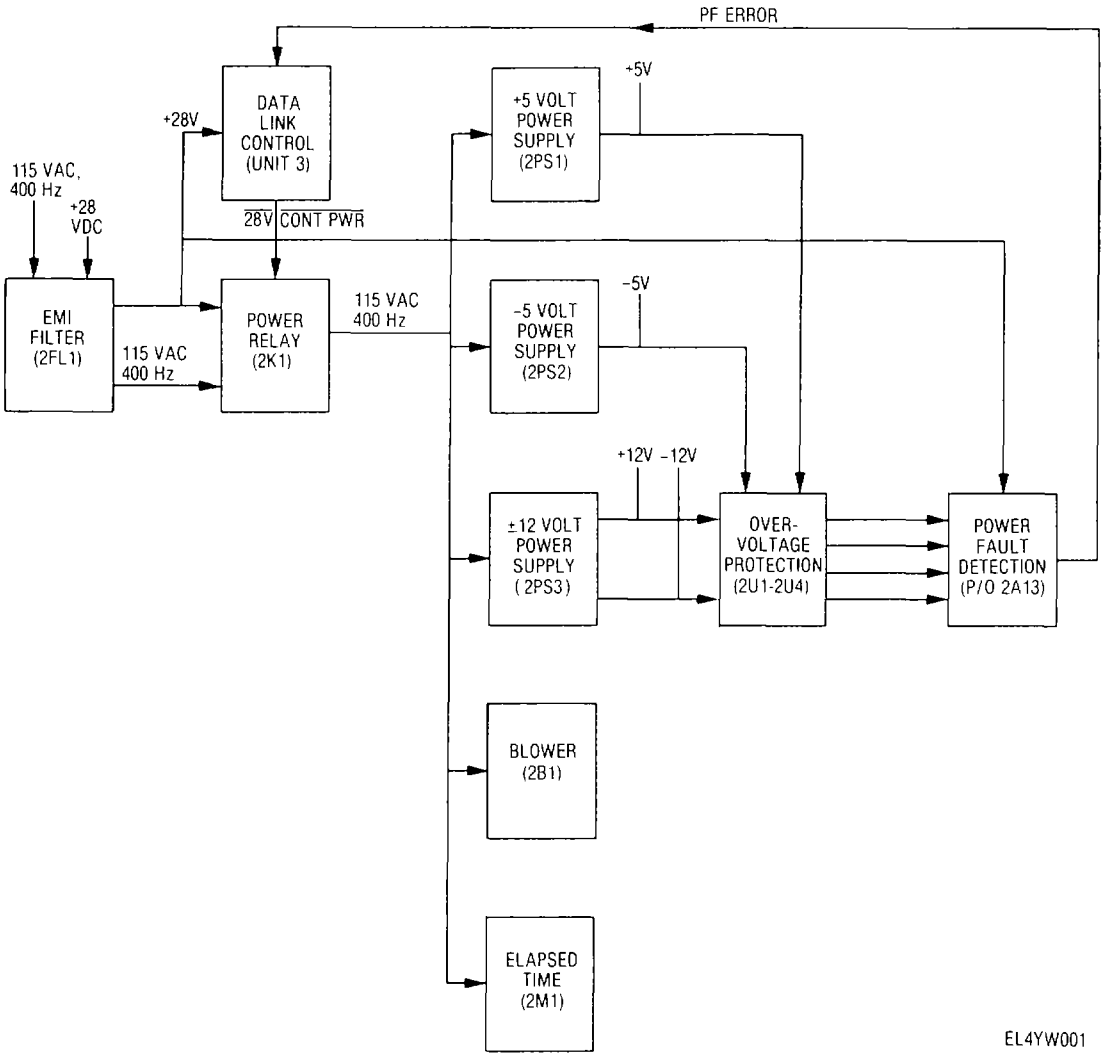


Figure 2-12. Encoding subsystem power supply and distribution block diagram.

Section III. FUNCTION OF DATA TRANSMITTING SUBSYSTEM

2-17. Uhf Receiver-Transmitter

The uhf receiver-transmitter receives and transmits FM-FSK data on any one of 7, 000 channels in the 225 000 to 399 975 MHz range Within the data transmitting set, the uhf receiver-transmitter primary function is to transmit serially encoded digital data to the ground station The receiver section is used only for monitoring the transmitted signal, of which a sample is supplied to the encoder for analysis Additional selfcheck circuitry is provided for determination of low rf power and synchronization failure The transmitter section power output is 30-watts continuous A detail functional description of the uhf receiver-transmitter is provided in TM 11-5841-286-13.

2-18. Uhf Radio Control

The uhf radio control provides uhf receiver-transmitter frequency/channel selection Two modes of frequency selection are provided manual and preset In the manual mode, frequency selection is accomplished by positioning individual digit selectors to the desired frequency In the preset mode, frequency selection is accomplished by a single channel selector switch Up to 20 channels may be selected in the preset mode

2-19. Uhf Radio Mount

The uhf radio mount receives 115 V ac, 400 Hz single phase and +28 V dc for application to the uhf receiver-transmitter The 115 V ac, 400 Hz is used only for operation of a rear-mounted cooing fan

CHAPTER 3

DIRECT SUPPORT MAINTENANCE INSTRUCTIONS

Section I. GENERAL

3-1. Introduction

Maintenance instructions presented in this chapter apply primarily to Encoder, Video KY-8651AKT-18B (encoder) and Control, Data Link C-10546/AKT-18B (data link control) Maintenance Instructions for Radio Set AN/ARC-164(V) 16 (uhf radio set) are given In TM 11-5841-286-13 The following maintenance duties are assigned to direct support maintenance personnel:

a. Testing encoder, datalink control, and uhf radio set to localize trouble to a faulty subassembly or chassis-mounted part

b. Replacing of faulty subassemblies or chassis-mounted parts

c. Performing power supply and overvoltage protector adjustments

d. Repairing of filter assembly 2FL1

WARNING

Be careful when 115 V ac is applied to the equipment Serious injury or DEATH may result from contact with terminals carrying this voltage

CAUTION

When making resistance measurements en-sure that power is removed from the unit being tested Failure to comply may result in erroneous readings or in damage to the equipment.

3-2. Voltage and Resistance Measurements

All procedures for making voltage and resistance measurements are contained in the troubleshooting procedures (section II)

3-3. Waveform Measurements

All procedures for making waveform measurements are contained in the troubleshooting procedures (section III)

Section II. TOOLS AND EQUIPMENT

3-4. Tools and Test Equipment Required

The tools and test equipment required for direct support maintenance are listed below

Test equipment	*Technical manual*	Common name
Multimeter ANfUSM-223	TM 11-6625-654-14	Multimeter
Oscilloscope AN/USM-281C	TM 11-6625-2658-14	Oscilloscope
Digital Voltmeter AN/GSM-64B	TM 11-6625-444-14-1	Digital voltmeter (DVM)
Power Supply PP-3940A/G	TM 11-6130-247-15	Low voltage power supply (LVPS)
Tool Kit, Electronic EquipmentTK-100/G	SG 5180-91-CL-S21	TK-10O/G
Tool Kit, Electronic Equipment TK-105/G	SG 5180-91-CL-R07	TK-105/G
Test Set, Electronic Systems ANIUKM-5	TM 11-6625-2937-13	Test set group

3-5. Materials Required

The materials required to perform direct support maintenance are listed m appendix B

Section III. TROUBLESHOOTING

3-6. General

This section contains information to aid in the direct support troubleshooting of the data transmitting set and each repairable subassembly The troubleshooting procedure comprises a list of tools and test equipment required, a test setup diagram, a functional test procedure, a troubleshooting table, and additional data as required Malfunctions listed in the troubleshooting table are assumed to occur during testing of the data transmitting set or its subassemblies The entire test procedure should be repeated after repair to make sure that the malfunction was corrected

3-7. Encoder and Data Link Control Troubleshooting

a. Tools and Test Equipment Required. The tools and test equipment required for troubleshooting the encoder and data link control are those in paragraph 3-4.

b. *Test Setup*. The encoder and data link control test setup is shown in figure 3-1. Perform the physical tests given in table 3-3 prior to connecting the equipment in the test setup.

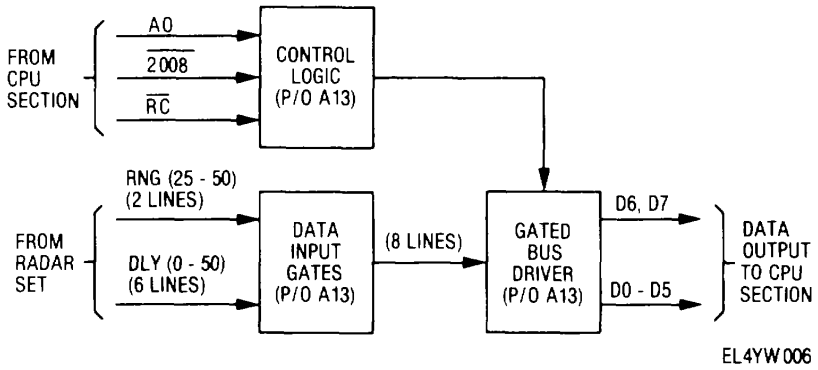


Figure 3-1. Encoder and data link control test setup.

c. *Preliminary Control Settings*. Set the equipment controls as follows prior to beginning the functional test procedures:

Control	*Setting*
Data link control:	
POWER	OFF
Test Set, Electronic Systems TS-3796/UKM-4 (control interface unit):	
POWER	OFF
MODE SELECT	UNIT TEST ENC

d. *Testing and Troubleshooting Procedures*. The first step in troubleshooting the encoder and data link control is to perform the functional test procedure given in table 3-1. Then, when a fault indication is obtained, locate the appropriate MALFUNCTION in table 3-2 and continue as directed by the TEST OR INSPECTION and CORRECTIVE ACTION columns of the table. Test the repaired circuit card or replacement circuit card or component before installing it in the encoder. Then retest the encoder with the repaired or new circuit card or component installed.

Table 3-1. Encoder and Data Link Control/Functional Test

Step no,	*Control settings*			*Performance standard*
	Test equipment	*Equipment under test*		
1	Control Interface unit: POWER switch: ON.	POWER switch: STBY.	*a.* Observe ENCODER and RT FAULT indicators on data link control. *b.* Observe encoder ELAPSED TIME *c.* Observe encoder ELAPSED TIME Meter	*a.* Indicators are off. *b.* Blower operates *c.* Meter operates as indicated by small tab pulsating in meter face
2		AIRBORNE BITE switch: Press down	Observe RT FAULT, ENCODER FAULT, and BITE IN PRCS indicator lamps on the data link control	RT FAULT and ENCODER FAULT indicator lamps illuminate for approximately3 seconds. And then go off. BITE IN PRCS indicator lamp stays illuminated 3 additional seconds and then go off

Table 3-1. Encoder an Data Link Control Functional Test

Step	Control Settings: Test Equipment	Control Settings: Equipment under test		Performance Standard
		POWER switch XMT DOWNLINK BITE switch Press down	Same as above	Indicator lamps sequence **is** as follows 1.RT FAULT, ENCODER FAULT, and BITE IN PRCS lamps illuminate 2.RT FAULT and ENCODER FAULT lamps 3.RT FAULT lamp illuminates m approx.- go off **in** approximately 3 seconds mately 3 seconds
4		Depress DOWNLINK BITE switch	Observe BITE IN PRCS indicator lamp RT on data link control	BITE IN PRCS indicator lamp is extinguished FAULT **remains** lluminated
5	POWER switch OFF	POWER switch OFF	Disconnect test setup	None

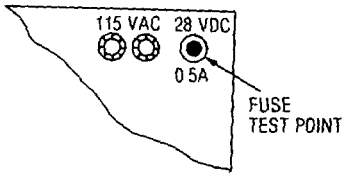
Table 3-2. Encoder and Data Link Control Troubleshooting

MALFUNCTION TEST OR INSPECTION CORRECTIVE ACTION

WARNING

DANGEROUS VOLTAGES EXIST IN THIS EQUIPMENT Be careful when working around the 115-volt ac lne-to-neutral connections

1. ENCODER FAN AND ELAPSED TIME METER DO NOT OPERATE ENCODER FAULT LIGHT NOT LIT
(Data link control POWER switch Is In STBY or XMIT)
Step 1. Check for 28 + volts dc at fuse test point on encoder front panel



(a) Voltage present. Go to step 3.
(b) Voltage absent Set UKM-4 POWER switch to OFF Replace fuse Set UKM-4 POWER switch to ON If fuse blows, go to step 5. Voltage absent and fuse is good, go to step 2.

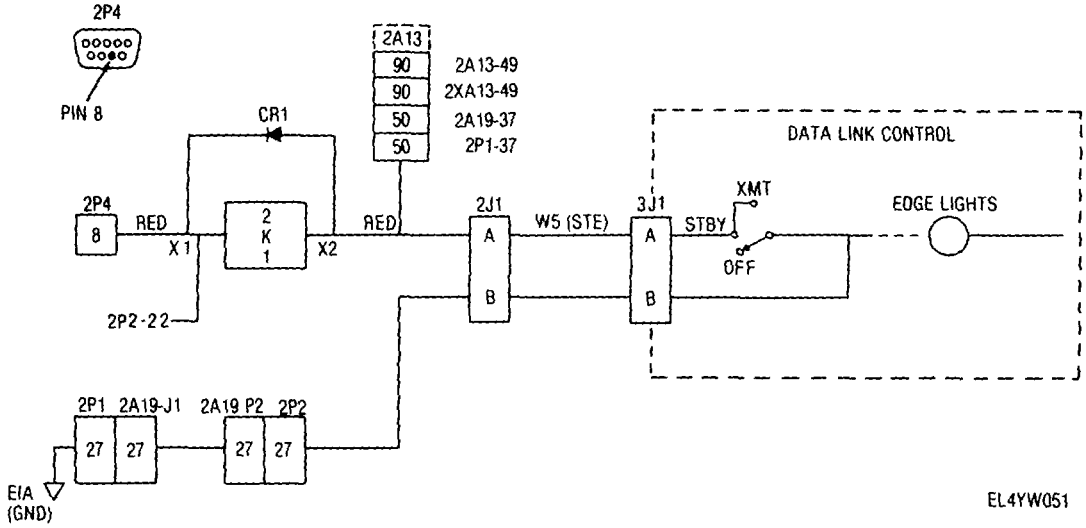
Step 2 Disconnect 2J2 Check for 28 _ 2 volts dc *between* pins D and C of UKM-4 cable connector
(a) Voltage not correct Refer to TM 11-6625-2937-13, Test Set, Electronles Systems ANfUKM-5 Check UKM-5 output voltage
(b) Voltage correct Set UKM-4 POWER switch to OFF Remove encoder 2FL1 (para 3-16) Refer to figure 3-4, sheet 7 Isolate faulty component or wiring Repair or replace components as necessary

Step 3 Set UKM-4 POWER switch to OFF Disconnect 2P4 from 2FL1-J 1 Set POWER switch to ON Measure 28 + 2 vdc betw, pins 2FL1-J1, pin 8 (+)and 2FL1-J1, pin 7 (gnd)
(a) Voltage present, go to step 4.
(b) Voltage incorrect Set UKM-4 POWER switch to OFF Remove 2FL1 (para 3-16) Using figure 3-4, sheet 4, isolate faulty component or wiring Repair wiring or replace faulty component as necessary

Step 4 Set UKM-4 POWER switch to OFF Using point-to-point diagram below and ohmmeter, isolate faulty component or wiring Repair wiring or replace components as necessary

Table 3-2. Encoder and Data Link Control Troubleshooting-Continued

MALFUNCTION TEST OR INSPECTION CORRECTIVE ACTION



Step 5 Set UKM-4 POWER switch to OFF Disconnect 2P4 from 2FL1-J1 Connect ohmmeter(X1 scale) between 2P4 pm 8 and chassis ground
- (a) Ohmmeter reads less than 100 ohms Go to step 4
- (b) Ohmmeter reads open or high resistance Remove 2FL1 (para 3-16) Use figure 3-6 to isolate faulty component Repair or replace as necessary

2. ENCODER OPERATES WITH DATA LINK CONTROL POWER SWITCH OFF

Step 1 Set UKM-4 POWER switch to OFF Remove circuit board 2A16(para 3-11) Set UKM-4 POWER switch to ON
- (a) Encoder no longer operates with data link control POWER switch at OFF Test circuit card 2A16 (para 3-36)
- (b) Encoder stall operates with data Ink control POWER switch set to OFF Set UKM-4 POWER switch to OFF Disconnect connector 2P4 from 2FL1 -J1 (para 3-16) Go to step 2

Step 2 With ohmmeter set on X 100 scale, measure resistance between 2E1A (gnd) and 2K1 -X2
- (a) Resistance more than 500 ohms Replace relay 2K1(fig 3-2)
- (b) *Resistance less* than 500 ohms Use the point-to point wiring diagram below and with ohmmeter isolate faulty component or wiring Repair or replace faulty component or wiring as necessary

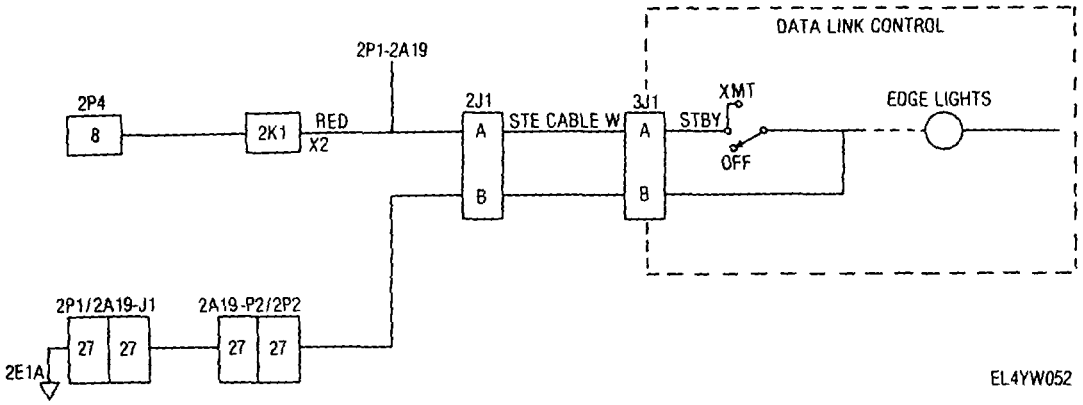


Table 3-2. Encoder and Data Link Control Troubleshooting-Continued

MALFUNCTION
TEST OR INSPECTION
CORRECTIVE ACTION

3. ENCODER FAN DOES NOT OPERATE AFTER PLACING DATA LINK POWER CONTROL SWITCH INTO STBY POSITION ELAPSED TIME METER OPERATES NORMALLY ENCODER FAULT LAMP OFF

WARNING
HIGH VOLTAGE
You will be measuring approximately 220 volts ac In the next step.
BE CAREFUL!

Step 1 Use multimeter to check for 220 + 20 Vac across terminals E8 and E9 just behind blower assembly (fig 3-2)
(a) Voltage correct Replace blower motor 2B1 (para 3-17)
(b) Voltage incorrect Go to step 2.
Step 2 Set UKM-4 POWER switch to OFF, label, then disconnect wires to 2B1-T4 and 2B1-T8 (fig 3-2) Be sure the wire ends are not touching each other or the encoder Measure resistance between 2E8 and 2E9 (fig 3-2)
(a) Approximately 200 ohms resistance (normal) Proceed to step 3
(b) Approximately zero ohms. Replace C1(para3-19)
Step 3 Check continuity of wire which was on 2B1-T4 to terminal 2E9 and wire which was on 2B1 -T8 to terminal 2E8
(a) No continuity Replace wire(s) Proceed to step 4
Step 4 Wrap bare ends of each of the two wires disconnected m Step 2 with electrical tape and reposition them so they will not short out on anything

WARNING
115 Vac may be present on 2E8, 2E9, 2B1-T1, and the wires loosened in step 2 above.

Step 5 Apply power to 2J2, turn on the encoder and measure the voltage from 2E9 to ground
(a) Zero volts (abnormal) Turn off and disconnect power, trace chassis wring from 2E9
(b) 115Vac(normal) Proceedtostep6
Step 6 Measure the voltage from 2E8 to chassis ground
(a) Zero volts Turn power OFF Replace 2C1 (para 3-19)
(b) 115 Vac Proceed to step 7
Step 7 Measure the voltage from 2E9 to 2B1-T1 (fig 3-2)
(a) 115Vac(normal) Turn power OFF Replace B1(para 3-17)
(b) Zero Vac Check continuity of wiring from 2B1-T1

4. ENCODER ELAPSED TIME METER DOES NOT OPERATE, BLOWER MOTOR OPERATES NORMALLY
Step 1 Using multimeter, check for 115 Vac across terminals of ELAPSED TIME meter 2M1 (fig 3-2)
(a) Voltage present Turn power OFF Replace2Ml (fig 3-2)
(b) Voltage absent Check continuity of wires to 2M1 (fig FO-4, table 3-8) Repair faulty wiring

5. ENCODER FAULT INDICATOR ON DATA LINK CONTROL ILLUMINATES IMMEDIATELY AFTER PLACING POWER SWITCH IN STBY POSITION, BUT ENCODER BLOWER DOES NOT OPERATE
Step 1 Turn POWER switch to OFF and check 115 volt 400 Hz fuses on encoder front panel
(a) Replace defective fuse(s) Proceed to step 2
(b) Fuses good Proceed to step 12
Step 2 Visually inspect wires (gray) carrying 115 Vac m encoder chassis These wires connect 2FL1 to 2K1 (input), 2K1 (output) to M1, B 1, PS2, and PS3 Replace defective wires Proceed to step 3
Step 3 Place POWER switch in STBY
(a) Encoder operates normally Fault has been corrected
(b) Malfunction 5 still exists Proceed to step 4
(c) Malfunction other than Malfunction 5 A symptomatic fault has been corrected Proceed to the new malfunction to find primary
Step 4 Turn power OFF If you had to replace defective 115 Vac 400 Hz fuses before, recheck them now Otherwise, proceed to step 12
(a) Disconnect power cable from 2J2 Replace defective fuses Proceed to step 5
(b) Fuses not defective Put them back m encoder Proceed to step 12
Step 5 Using multimeter, check for a short circuit between 2Kl-A2 and 2K1-Bi
(a) No short circuit Proceed to step 7
(b) Short circuit proceed to step 6
Step 6 Disconnect 2P4 from 2FLIJ 1 and check again for a short circuit between 2K1-A2 and 2K1-B2
(a) Still short circuited Repair wiring between 2P4 and 2K1 and/or replace 2K1 as necessary
(b) Not short circuited Remove and repair 2FL1 (fig 3-6) The 115 Vac circuit In 2FL1 is at fault
Step 7 Check for a short circuit between 2K1-A1 and 2Kl-B1 (use R x 100 scale A normal reading is 200 ohms to 500 ohms through the power supply windings)
(a) No short circuit Replace relay 2K1
(b) Short circuit Proceed to step 8

Table 3-2. Encoder and Data Link Control Troubleshooting-Continued

MALFUNCTION
TEST OR INSPECTION
CORRECTIVE ACTION

Step 8 Label, then disconnect, the three wires at blower connecting 2B1 to terminals 2E8, 2E9, and 2E10 Check **if** 2K1-A1 is still shorted to 2Kl-B1
(a) To short circuit Proceed to step 9
(b) Shortcurcuit Proceed to step ll
Step 9 Check 2C1 for a short circuit (2E8 to 2E9)
(a) No short circuit Remove defective 2B 1 and replace with good blower Reconnect wires
(b) 2C1 short circuited Replace defective 2C1 Reconnect 2B1 Proceed to step 10
Step 10 Check for short circuit between 2K1-A1 and 2K1-B1
(a) No short circuit Fault was corrected with replacement of 2C1
(b) Stdl shorted Remove defective blower 2B1 Replace with good blower Reconnect wires
Step 11 With power OFF, unsolder 115 Vac leads to 2M1 and recheck for short circuit between 2K1-A1 and 2K1-B1 Repeat this procedure on 2PS1, 2PS2, and 2PS3 until short circuit between disappears Replace the short circuited component (the last one unsoldered) and reconnect the others If all these components are disconnected and a short circuit still exists, replace 2K1
Step 12 Reconnect power cable to 2J2 Turn power ON Check for 115 Vac between K1-A2 and K1-B2
(a) Voltage absent Proceed to step 13
(b) Voltage present Proceed to step 15
Step 13 Turn power OFF Disconnect 2P4 from 2PL1 Turn power ON and check for 115 Vac across 2FL1J1-5 to FL1J1-4 (fig 3-6)
(a) Voltage absent Turn power OFF Remove and repair 2FL1 Ac circult s defective
(b) 115Vacpresent Proceedtostepl4
Step 14 Check ac wiring from 2FL1 to 2K1
(a) Turn power OFF Replace any defective wiring
(b) No defective wiring Turn power OFF Replace 2K1
Step 15 Disconnect power cable from 2J2 Return to step 7

6. ENCODER FAULT INDICATOR ON DATA LINK CONTROL ILLUMINATES IMMEDIATELY AFTER PLACING POWER SWITCH IN STBY POSITION AND ENCODER BLOWER OPERATES
Step 1 Measure dc voltage at 2A13J1-5
(a) 3 5 + 1 5V present Perform step 2
(b) 0 ± 0 5V present Proceed to step 3
Step 2 Turn power OFF Remove 2A16 Reapply power and measure the voltage at 2A13J1-7
(a) 0 ± 0 5V present Turn power OFF Replace 2A16
(b) Any other voltage present Turn power OFF Replace defective 2A13
Step 3 Measure dc voltage at 2A13J1-3
(a) 10 + 1 Vdc(normal) Proceed to step 4
(b) Any other voltage Turn power OFF Replace defective 2A13
Step 4 Measure dc voltage at 2A13J1-1
(a) + 12 + 0 6 Vdc (normal) Proceed to step 13
(b) Any other voltages Proceed to step 5
Step 5 Check for + 12 $^{+}$ 0 6 Vdc at 2PS-3 to 2PS-4 (gnd)(fig 3-7)
(a) + 12 ± 0 6 Vdc Proceed to step 6
(b) Any other voltage Proceed to step 8
Step 6 Check for + 12 ± 0 6 Vdc at 2A19XA13-2
(a) + 12 + 0 6 Vdc Turn power OFF Remove 2A13 and check continuity between 2A19XA13-54 and 2A19XA13-50 If open, replace 2A19 If not, replace 2A13
(b) Any other voltage Proceed to step 7
Step 7 Turn power OFF Disconnect 2P3 from 2A19J3 Turn power ON Measure dc voltage at 2P3-A2
(a) + 12 + 0 6 Vdc Turn power OFF Replace electrical connector assembly 2A19
(b) Any other voltage Turn power OFF Repair wiring from 2PS3-3 to 2P3-A2 or from 2PS3-4 to ground Reconnect 2P3 to 2A19J3
Step 8 Turn power OFF Pull out all circuit cards far enough to break contact with connectors on electrical connector assembly 2A19 Turn power ON Adjust 2PS3 overvoltage protectors 2U3 and 2U4 (para 3-21)

NOTE
Make only those adjustments pertaining to 2PS3, 2U3, and 2U4.

(a) Adjustment successful Proceed to step 9
(b) Adjustment unsuccessful Proceed to step 11
Step9 Turn power OFF Insert circuit cards in connectors Turn power ON
(a) Encoder fault lamp no longer illuminates with power switch m STBY Fault is corrected
(b) Encoder fault lamp still lights immediately In STBY Proceed to step 10
Step 10 Either power supply 2PS3 is unable to deliver rated load or a shorted circuit card Is overloading supply Turn power OFF Check each circuit card for short circuits per para 3-27 through 3-37 to point where MODE/POWER SHORT lamp Is checked (Full functional test of each card is not necessary) Replace any defective cards
Step 11 Isolate + 12V supply 2PS3 by labeling and disconnecting wires from terminal 3, 4, and 5 Turn power ON Adjust ADJ pot on 2PS3 for + 12 + 0 1V (2PS3-3 to 2PS3-4 which is ground)

Table 3-2. Encoder and Data Link Control Troubleshooting--Continued

MALFUNCTION TEST OR INSPECTION CORRECTIVE ACTION

(a) Correct voltage not present Turn power OFF Replace 2PS3
(b) Correct voltage not present prior to adjustment but was obtained Turn power OFF Reconnect wires to 2PS3-3, -4, and -5 Turn power ON Retest encoder
(c) Correct voltage prior to adjustment Either 2U3 or 2U4 Is defective Proceed to step 12

Step 12 Turn power OFF Connect proper wires to 2PS3-3 and 2PS3-4 Measure dc voltage across 2PS3-3 and 2PS3-4 with POWER switch set to STBY
(a) + 12 + 0 1 Vdc Turn power OFF Check wiring to 2U4 Replace 2U4 if wiring good Turn power ON Adjust 2U4 (para 3-21)
(b) Any other voltage Turn power OFF Check wiring to 2U3 Replace 2U3 If wiring is good Turn power ON Adjust 2U3 (para 3-21)

Step 13 Compare voltage at 2A13J1-A with 2A13J1-B
(a) A less than B (normal) Proceed to step 18
(b) B less than A Proceed to step 14

Step 14 Measure voltage across 2PS3-5 to 2PS3-4 (ground) (fig 3-7)
(a) 12 + 0 6 Vdc Perform step 15
(b) Any other voltage Perform step 17

Step 15 Check for - 12 Vdc at 2A19XA13-51
(a) -12 + 0 6 Vdc Turn power OFF Replace 2A13
(b) Any other voltage Perform step 16

Step 16 Turn power OFF Disconnect 2P2 from 2A19J2 Turn power ON Measure dc voltage at 2P2 -19
(a) - 12 + 0 6 Vdc Turn power OFF Replace electrical connector assembly 2A19
(b) Any other voltage Turn power OFF Repair wiring from 2PS3-5 to 2P2-19 Reconnect 2P2 to 2A19J2

Step 17 Turn power OFF Pull out all circuit cards far enough to break contact with 2A19 Turn power ON Adjust 2U3 and 2U4 (para 3-21)

NOTE

Make only adjustments pertaining to 2PS3, 2U3, and 2U4.

(a) Adjustment successful Perform step
(b) Adjustment unsuccessful Turn power OFF Replace 2PS3 Note that - 12 Vdc output of 2PS3 is not independent of + 12 Vdc out-put, therefore, any malfunctions of 2U3 or 2U4 would have been corrected earlier at steps 11 and 12

Step 18 Turn power ON Measure dc voltage at 2A13J1-6
(a) + 5 ± 0 25 Vdc Perform step 25
(b) Any other voltage Perform stepl9WARNING

WARNING

DANGEROUS VOLTAGES EXIST IN THIS EQUIPMENT MAKE SURE POWER IS OFF BEFORE DISASSEMBLING.

Step 19 Remove cover from 2PS1 (fig 3-4, sheet 1 and sheet 3) Turn power ON Measure dc voltage between 2PS1-3 and 2PS1-4 (ground)(fig 3-7)
(a) + 5 + 0 25 Vdc (normal) Perform step 20
(b) Any other voltage Performstep23

Step20 Check for + 5 Vdc at 2A19XA13-43
(a) + 5 ± 0 25 Vdc Perform step 21
(b) Any other voltage Perform step 22

Step 21 Turn power OFF Remove 2A13 Check contmmuity from 2A19XA13-86 to -52
(a) Continuity Replace2A13
(b) Open circuit Replace2A19

Step 22 Turn power OFF Disconnect 2P3 from 2A19J3 Turn power ON Measure dc voltage at 2P3-A3 and A4
(a) + 5 + 0 25 Vdc Turn power OFF Replace 2A19
(b) Any other voltage at either -A3 or -A4 Turn power OFF Repair wiring from 2PS1-3 to 2P3 or from 2PS1-4 to ground Reconnect

Step 23 Turn power OFF Pull out all circuit cards far enough to break contact with connectors on 2A19 Turn power ON Adjust 2PS1 and 2U1 (para 3-21)

NOTE

Make only those adjustments pertaining to 2PS1 and 2U1

(a) Adjustment successful Perform step 24
(b) Adjustment unsuccessful Perform step 33

Step 24 Perform steps 9 and 10 above but substitute "2PS1" for "2PS3" In the step 10 procedure

Step 25 Compare the voltage at 2A13J1-4 with 2A13J1-C
(a) C higher than 4 (normal) Turn power OFF Replace 2A13
(b) 4 higher than C Perform step 26

Step 26 Measure dc voltage across 2PS2- 3 (ground) to 2PS2-4 (- 5 Vdc) (fig 3-7)
(a) - 5 + 0 25 Vdc Perform step 27
(b) Any other voltage Perform step 303-7

Table 3-2. Encoder and Data Link Control Troubleshooting-Continued

MALFUNCTION
TEST OR INSPECTION
CORRECTIVE ACTION

Step 27 Check for - 5 Vdc at 2A19XA13-1
(a) - 5 + 0 25 Vdc Perform step 28
(b) Any other voltage Perform step 29
Step 28 Turn power OFF Remove 2A13 Check continuity from 2A19XA13-48 to -53
(a) Continuity Replace2A13
(b) No continuity Replace2A19
Step 29 Disconnect 2P3 from 2A19J3 Turn power ON Measure dc voltage at2P3-A1
(a) - 5 + 0 25 Vdc Turn power OFF Replace 2A19
(b) Any other voltage Turn power OFF Repair wiring from 2PS2-4 to 2P3 or from 2PS2-3 to ground Reconnect 2P3 to 2A19J3
Step 30 Turn power OFF Pull out all circuit cards far enough to break contact with connectors on 2A17 Turn power ON Adjust 2PS2 (para 3-21)
(a) 2PS2 adjusts Perform steps 9 and 10 above but substitute 2PS2 for 2PS3 In the step 10 procedure
(b) 2PS2 does not adjust Perform step 31
Step 31 Turn power OFF Test each circuit card for short circuits using STE
(a) Replace defective circuit cards
(b) All Circut cards check out good Perform step 32
Step 32 Disconnect wires from 2PS2-3 and -4 Turn power ON Measure 2PS2-4 (- 5 volts) to 2PS2-3 (ground)
(a) - 5 ± 0 25 Vdc Turn power OFF Check wiring to 2U2 and replace 2U2 if wiring is good
(b) Any other voltage Perform step 33
Step 33 Adjust 2PS2 for - 5V + 0 25 Vdc
(a) Supply adjust Reconnect and retest encoder
(b) Does not adjust Turn power OFF Replace 2PS2
Step 34 Turn power OFF. Isolate + 5 Vdc supply 2PS1 by disconnecting wires from terminals 2PS1-3 ans 2 PS1-4. Turn power ON. Adjust ADJ pot 2PS3 for + 5 + 0 1 Vdc measured from 2PS1-3 to 2PS1-4 (ground)
(a) Specified voltage not obtained Turn power OFF Replace 2PS3
(b) Voltage was not + 5 ± 0 25 Vdc prior to adjustment, but specified voltage was obtained Reconnect wires to 2PS1-3 and 2PS1-4 Retest encoder
(c) Voltage was + 5 + 0 25 Vdc prior to adjustment Turn power OFF Check wiring to 2U1 Replace 2U1 If wiring is good Adjust new test encoder

7. ALL INDICATORS ON DATA LINK CONTROL REMAIN OFF AFTER AIRBORNE OR DOWNLINK BITE SWITCH IS PRESSED, BUT ENCODER BLOWER OPERATES NORMALLY
Step 1 Check data link control AIRBORNE BITE switch 3S2 and DOWNLINK BITE switch 3S3 and associated wiring for operation and continuity Replace or repair defective wiring
Step 2 Test each encoder circuit card per paragraph 3-26 Test circuit cards m following order 2All, 2A14, 2A7, 2A9, 2A13 (para 3-34a through 3-34c, (8) only), 2A16, 2A12, 2A5, 2A6, 2A4, 2A3, and 2A17
Step 3 Test connector assembly 2A19 by replacement (para 3-15)
8. ONE OR MORE (BUT NOT ALL) BITEIN-PRCS, ENC FAULT, OR RT FAULT INDICATORS DO NOT MOMENTARILY ILLUMINATE AFTER AIRBORNE BITE SWITCH IS PRESSED
Step 1 Check unit bulb(s) Replace if defective Recheck
Step 2 Turn power OFF Check circuit card 2A16 (para 3-36) Replace defective crcuit card (para 3-11)
Step 3 Check wiring associated with lamps in data link control and encoder chassis Repair faulty wiring or replace electrical connector
9. ENCODER FAULT INDICATOR REMAINS ILLUMINATED AFTER COMPLETION OF AIRBORNE BITE TEST (LIGHT MAY GO OFF MOMENTARILY DURING TEST)
Step 1 Check for a logic high (3 5 1 5 Vdc) at the following pmins on 2A13J1 (fig 3-2, detail A) If logic high is obtained, go to the related step In the table below An AIRBORNE BITE must be run once to set the Error Sources

2A 13J1 Pin No	*Related Step No*	*Error Source*
16	2	ADAS interface
17	3	Output/RCVR Interface
18	7	FT video
19	4	Drift angle
P	7	MT video
R	5	Film speed
T	6	Video ID

Perform the step(s) below When a defective card is found, replace It and retest the encoder
Step 2 Test 2A16 (para 3-36), 2A13 (para 3-34a through 3-34c (8)) in order Perform steps 2 and 3 of Malfunction 7 without repetition. Replace defective circuit card (para 3-11)
Step 3 Test 2A12 (para 3-33), 2A17 (para 3-37a through 3-37c (9), and 2A13 (para 3-34a through 3-34c (8)) m order Perform steps 2 and 3 of Malfunction 7 without repetition Replace defective circuit card (para 3-11)

Table 3-2. Encoder and Data Link Control Troubleshooting-Continued

MALFUNCTION TEST OR INSPECTION CORRECTIVE ACTION

Step4 Test 2A13 (para 3-34 in its entirety), 2A9 (para 3-31), and 2A5 (para 3-29) in order Perform steps 2 and 3 of Malfunction 7 without repetition Replace defective circuit card (para 3-11)

Step 5 Test 2A16 (para 3-36), 2A13 (para 3-34a through 3-34c (8)) and 2All (para 3-32) m order Perform steps 2 and 3 of Malfunction 7 without repetition Replace defective Circut card (para 3-11)

Step 6 Test 2A9 (para 3-31), 2A7 (para 3-30), 2A14 (para 3-35), and 2A13 (para 3-34a through 3-34c (8)) mn order Perform steps 2 and 3 of Malfunction 7 without repetition Replace defective circuitcard

Step7 Set oscilloscope to 50microsecondsper division, normal triggered, on positve-going edges Monitor 2A13J1-15. Press AIRBORNE BITE switch on data link control

(a) The oscilloscope trace remains low throughout the BITE test(does not trigger) The logic level at pm 15 is low (LO)
(b) The oscilloscope triggers and remains high (3 5+ 1 5V) without interruption, the level at pm 15 is high (HI)
(c) The oscilloscope trace may show a COMBINATION of HI and LO at pm 15

PIN 15 WAVEFORM (NOT NECESSARILY AS SHOWN)

Refer to the following table to determine the next step. For pm 15, HI, LO, and COMBINATION are as defined above; for **pms** 18 and

		Logiclevel at2A13J1pin	*Step (below)*			*Logic level at2A13J1 pin:*	*Step (below)*
18	P	15		18	P	15	
HI	LO	LO	9	LO	HI	COMBINATION	**15**
HI	LO	HI	8	HI	HI	LO	18
HI	LO	COMBINATION	10	HI	HI	HI	19
LO	HI	LO	13	HI	HI	COMBINATION	20

Step 8 Test 2A3 (para 3-28), 2A9 (para 3-31), and 2A2 (para 3-27) *in* order Perform steps 2 and 3 of Malfunction 7 without repetition Replace defective circuit card (para 3-11)

Step9 Test 2A4 (para 3-28), 2A9 (para 3-31), and 2A2 (para 3-27) in order Perform steps 2 and 3 of Malfunction 7 without repetition Replace defective circuit card (para 3-1 1)

Step 10 Set oscilloscope for 0 2V per division and 50 microseconds per division Monitor (2A17JI-17 Place POWER switch on data limk Replace defective circuit card ("ars 3-11)

(a) A pattern of pulses approximately 0 4 V in amplitude referenced to ground, each pulse approximately 13 microseconds wide, appears Test 2A9 (para 3-31), 2A7 (para 3-30), then 2A2 (para 3-27) Perform steps 2 and 3 of Malfunction 7 without repetition
(b) The pattern described in step 30(a) does not appear at any time Perform step 11

Step 11 Connect oscilloscope to 2A19XA17-26 Observe digital activity A pulse tram of normal logic levels (O± 0 5 V low level and Replace defective circuit d card (para 3-11) 3 5±1 5V high level with pulsewidths of approximately 13 microseconds should appear

(b) Correct pulses not present Test 2A7 (para 3-30), then 2A6 (para 3-29) Perform steps 2 and 3 of Malfunction 7 without repetition
(a) Correct pulse levels and widths are present, perform step 12.

Step 12 Check 2A19XA17-27 for a logic high level This signal cycles on and off during BITE You must restart by pressing DOWNLINK BITE once to terminate BITE and once again after the green BITE-IN-PRCS light goes out The high level should appear Replace defective circuit card within 2 or 3 seconds after restarting the BIT test The level will then go low momentarily and return high again

(a) Signal is always low or does not reach a true high level Test 2A 16 (para 3-36), then 2A17 (para 3- 37) Perform steps 2 and 3 of Malfunction 7
(b) Signal alternates high and low during BITE test Test 2A17 (para 3 -37) Perform steps 2 and 3 of Malfunction 7 without repetition Replace defective circuit card

Step 13 Test 2A6 (para 3-29), 2A9 (para 3-31), 2A7 (para 3-30), 2A4 (para 3-28), then 2A2 (para 3-27) Perform steps 2 and 3 of Malfunction Replace defective circuit card (para 3-11)

Table 3-2. Encoder and Data Link Control Troubleshooting-Continued

MALFUNCTION TEST OR INSPECTION CORRECTIVE ACTION

Step 14 Test 2A5 (para 3-29), 2A9 (para 3-31), 2A7 (para 3-30), 2A3 (para 3-28), then 2A2 (para 3-27) Perform steps 2 and 3 of Malfunction 7 Replace defective circuit card.

Step 15 Set oscilloscope to 0 2 V per division and 50 microseconds per division Connect scope to 2A17J1-S Place data lhnk control POWER switch to XMT and press DOWNLINK BITE switch

(a) A pattern of pulses approximately 0 8 volts m amplitude referenced to ground, pulse width approximately 6 microseconds IS observed Test 2A9 (para 3-31), 2A7 (para 3-30), then 2A2 (para 3-27)

Perform steps 2 and 3 of Malfunction 7

(b) The pattern described m step 15(a) does not appear at any timune Perform step 16

Step 16 With oscilloscope observe digital activity at 2A19XA17-28 A pulse tram of normal logic level (O+ 0 5 V low level and 3 5 + 1 5 V high level) with pulse widths of approximately 6 microseconds should be observed

(a) Correct pulse levels and widths are present, perform step 17

(b) Correct pulses not present Test 2A7 (para 3-30), then 2A6 (para 3-39) Perform steps 2 and 3 of Malfunction 7 Replace defective circuit card

Step 17 Check 2A19XA17-25 for a high logic level You may have to restart BITE as described in step 12

(a) Signal always low or does not reach a true high level Test 2A16 (para 3-36), then 2A17 (para 3-37) Perform steps 2 and 3 of Malfunction 7 Replace defective circuit card

(b) The signal alternates high and low during BITE test Test 2A 17 (para 3-37) Perform steps 2 and 3 of Malfunction 7 Replace defective crcuit card (para 3-11)

Step 18 Test 2A6 (para 3-29), then 2A7 (para 3-30) Perform steps 2 and 3 of Malfunction 7 Replace defective circuit card

Step 19 Test 2A5 (para 3-29), then 2A7 (para 3-30) Perform steps 2 and 3 of Malfunction 7 Replace defective circult card

Step 20 With DVM, measure voltage at 2A2J1- 1 (2A2J1-22 ground)

(a) 40 ± 0 **1** volts Perform step21

(b) Any other voltage Replace2A2(para3-11)

Step 21 With oscilloscope set to 0 2 V per division and 50 microseconds per division, observe 2A17J1-17 Place data link control POWER switch to XMT and press DOWNLINK BITE switch

(a) A pattern of pulses 0 4 V m amplitude referenced to ground each pulse approximately 13 microseconds **wide** observed Test 2A9 (para 3-31), 2A7(para 3-30), then 2A2 (para 3-27) Perform steps 2 and 3 of Malfunction 7

Replace defective circuit card

(b) Above pulses not present Perform step 22

Step 22 With oscilloscope observe digital activity at 2A19XA17-26 A pulse tram of normal logic levels (0 + 0 5 V low level and 3 5 + 1 5 V high level) with pulse widths of approximately 13 microseconds should be observed

(a) Correct pulse levels and widths are present Perform step 23

(b) Correct pulses not present Test 2A7, 2A6, 2A5, 2A17 in order Perform steps 2 and 3 of Malfunction 7

Step 23 Check 2A19XA17-35 and - 19 for a logic high while BITE is in process

(a) High not present (either or both points low) Test 2A16, then 2A17 Perform steps 2 and 3 of Malfunction 7 Replace defective circuit card (para 3-11)

(b) Both points high Test 2A17 Perform steps 2 and 3 of Malfunction 7

NOTE

Make sure power is off when removing and replacing circuit boards.

10. AIRBORNE OR DOWNLINK BITE CYCLE ABNORMAL OR BITE CYCLE NORMAL EXCEPT FAILS TO STAY IN BITE WHEN IN DOWNLINK BITE IN XMT

Step 1 Check 2A19XA16-37 for 0 + 0 5 volt

(b) Approximately 20 Vdc Turn power OFF Trace wiring from 2A19XA16P1-37 through 2A19J2-12, 2J1-D to encoder control 3J1-D to 3S1B-3 Repair defective wiring or replace 3S1 as necessary

Step2 For all other abnormal BITE cycles Test in order-2All (para 3-32), 2A13 (para 3-34a through 3-34c(8)), 2A12 (para 3-3), 2A14 (para 3-35), 2A7 (para 3-30), 2A5 (para 3-29), 2A6 (para 3-29), 2A9 (para 3-31), 2A16 (para 3-36), 2A3 (para 3-28), 2A4 (para 3-28), 2A17 (para 3-37) Replace connector 2A19 (para 3-15)

11. NO ERROR DETECTED, BUT ENCODER DOES NOT OPERATE PROPERLY WHEN INSTALLED IN AIRCRAFT

Step 1 If you have no additional information, test in following order

(a) 2A7 (para 3-30), 2A14 (para 3-35), 2All (para 3-32), 2A5 (para 3-29), 2A6 (para 3-29), 2A16 (para 3-36), 2A17 (para 3-37), 2A13 (para 3-34), 2A12 (para 3-33), 2A3 (para 3-28), 2A4 (para 3-28), 2A9 (para 3-31), 2A2 (para 3-27) Replace defective **circuit** card (para 3-11)

(b) Perform continuity checks for chassis wiring Repair wiring as necessary

(c) Check connector assembly 2A 19 by replacement (para 3-15)

(d) If additional information is available, test as Is appropriate,

Table 3-2. Encoder and Data Link Control Troubleshooting- Continued

MALFUNCTION TEST OR INSPECTION CORRECTIVE ACTION
Step 2 Radar range and/or delay error present Test 2A13 (para 3-34), 2All (para 3-32) Check chassis wiring Repair or replace as necessary Step 3 Drift angle error present Test 2A13 (para 3-34), 2A9 (para 3-31), 2A5 (para 3-29) Check chassis wiring Repair or replace as necessary Step 4 Ground speed error present Test2A16 (para 3-36), 2All (para 3-32) Check chassis wiring Repair or replace as necessary Step 5 ADAS error present Test2A16 (para 3-36), 2All (para 3-32) Check chassis wiring Repair or replace as necessary Step 6 Only FT video errors present Test 2A3 (para 3-8), 2A4 (para 3-28), 2A17 (para 3-37), 2A9 (para 3-31), 2A7 (para 3-30), 2A5 (para 3-29), 2A6 (para 3-29), and 2A14 (para 3-35) , and 2A2 (para 3-27) in order Step 7 Only MT video errors present Test 2A5 (para 3-29), 2A6 (para 3-29), 2A17 (para 3-37), 2A9 (para 3-31), 2A7 (para 3-30), 2A14 (para 3-35), and 2A2 (para 3-27) m order Repair or replace as necessary Step 8 Both FT and MT errors present Test 2A17 (para 3-37), 2A9 (para 3-31), 2A14 (para 3-35), 2A7 (para 3-31), 2A5 (para 3-29), 2A6 (para 3-29), 2A2 (para 3-27) **In** order Repair or replace as necessary Step 9 Abnormal fm spectrum from data transmitter present(with known good UHF receiver-transmitter) Test 2A17 (para 3-27) Repair or replace as necessary Step 10 Receive-transmitter errors present (with known good UHF receiver-transmitter) Test 2A17 (para 3-37), 2A12(para 3-33) Repair or replace as necessary
12. ALL OTHER MALFUNCTIONS Perform steps 2 and 3 of Malfunction 7

3-8. Uhf Radio Set Troubleshooting

Refer to TM11-5841-286-13 for uhf radio set troubleshooting procedures.

Section IV. MAINTENANCE OF TRANSMITTING SET, RADAR DATA AN/AKT-18B

3-9. General

The following paragraphs contain maintenance instructions for the encoder and data hnk control, including removal and replacement procedures, filter repair, cleaning, adjustment and repainting instructions. Refer to TM 11-5841-286-13 for maintenance of Radio Set AN/ARC- 164(V) 16.

3-10. Removal and Replacement Procedures.

Paragraphs 3-11 through 3-19 contain procedures for removal and replacement of encoder subassemblies and chassis-mounted parts on the encoder and data link control Figures 3-4 and 3-5 show the location of all components referenced m the removal and replace-ment procedures. Only standard hand tools supplied with Tool Kits, Electronic Equipment TK-100/G and TK-105/G are required to accomplish the removal and replacement procedures.

WARNING

Disconnect power from the equipment before performing removal or replacement procedures Failure to comply could result in electrical shock injury to personnel or dam-age to the equipment.

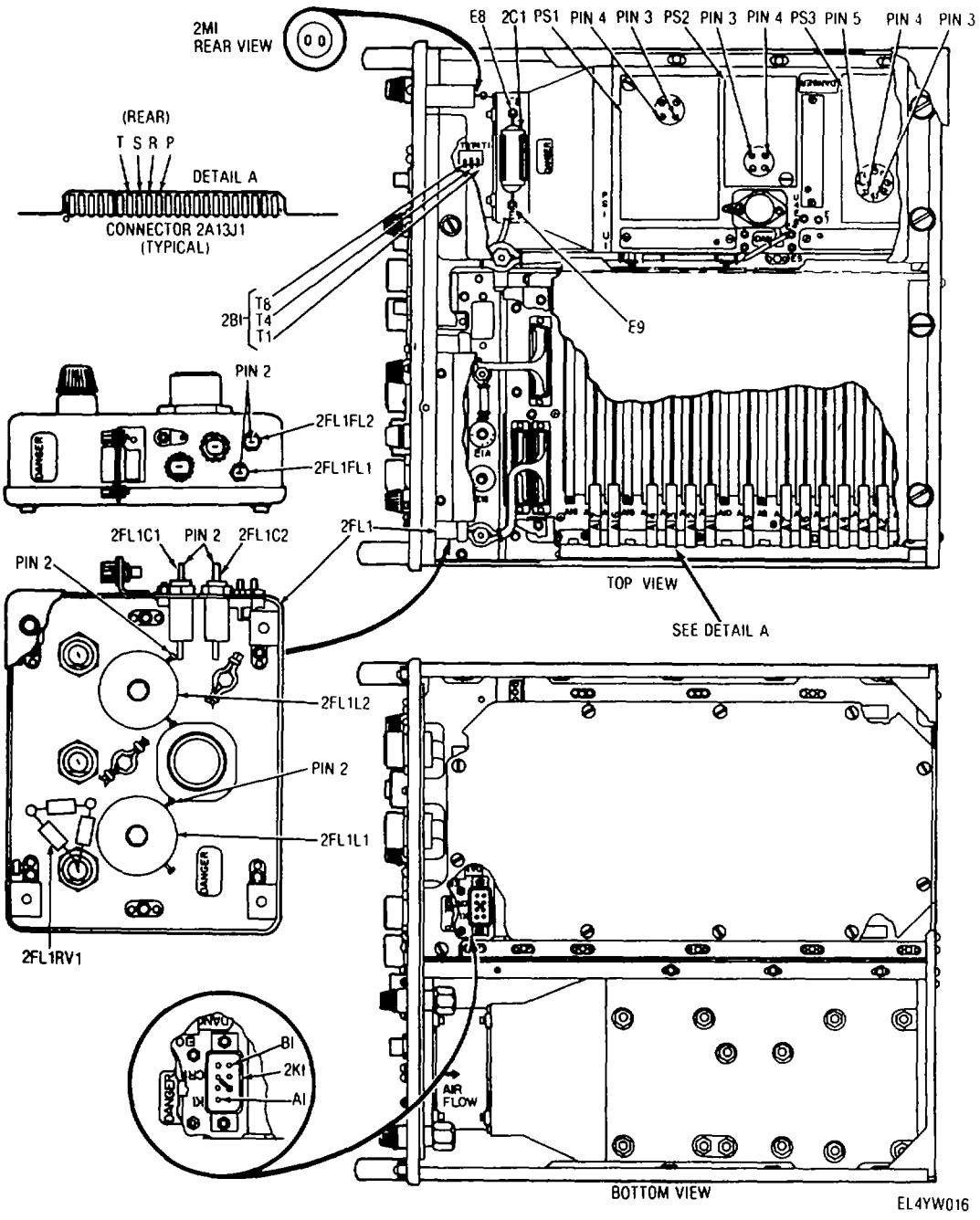


Figure 3-2. Encoder test point locations.

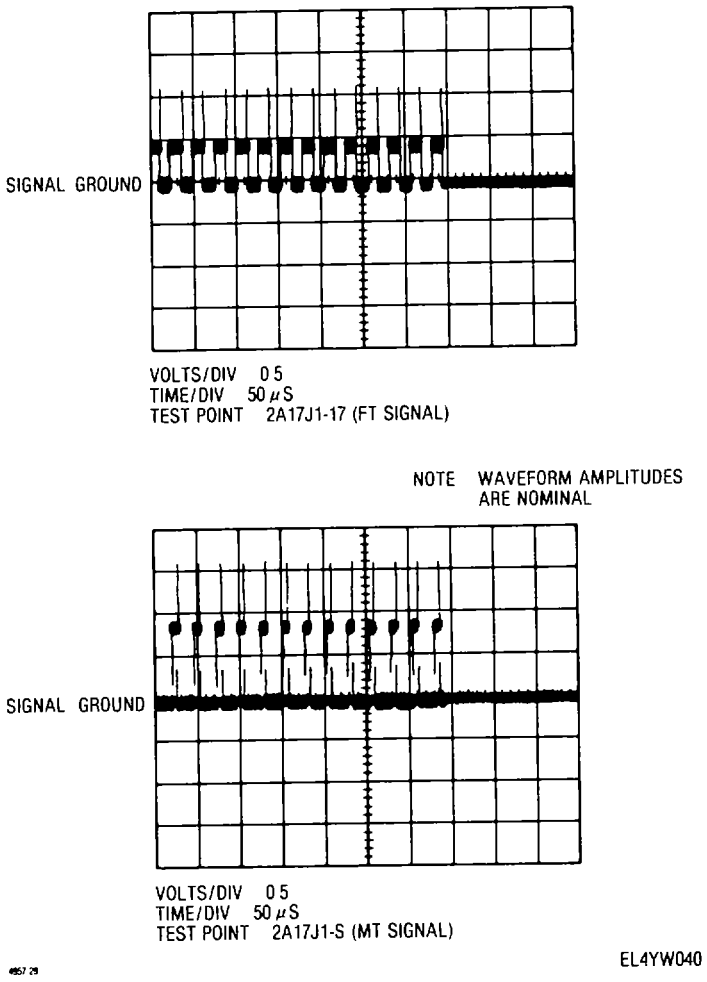


Figure 3-3. Encoder waveforms.

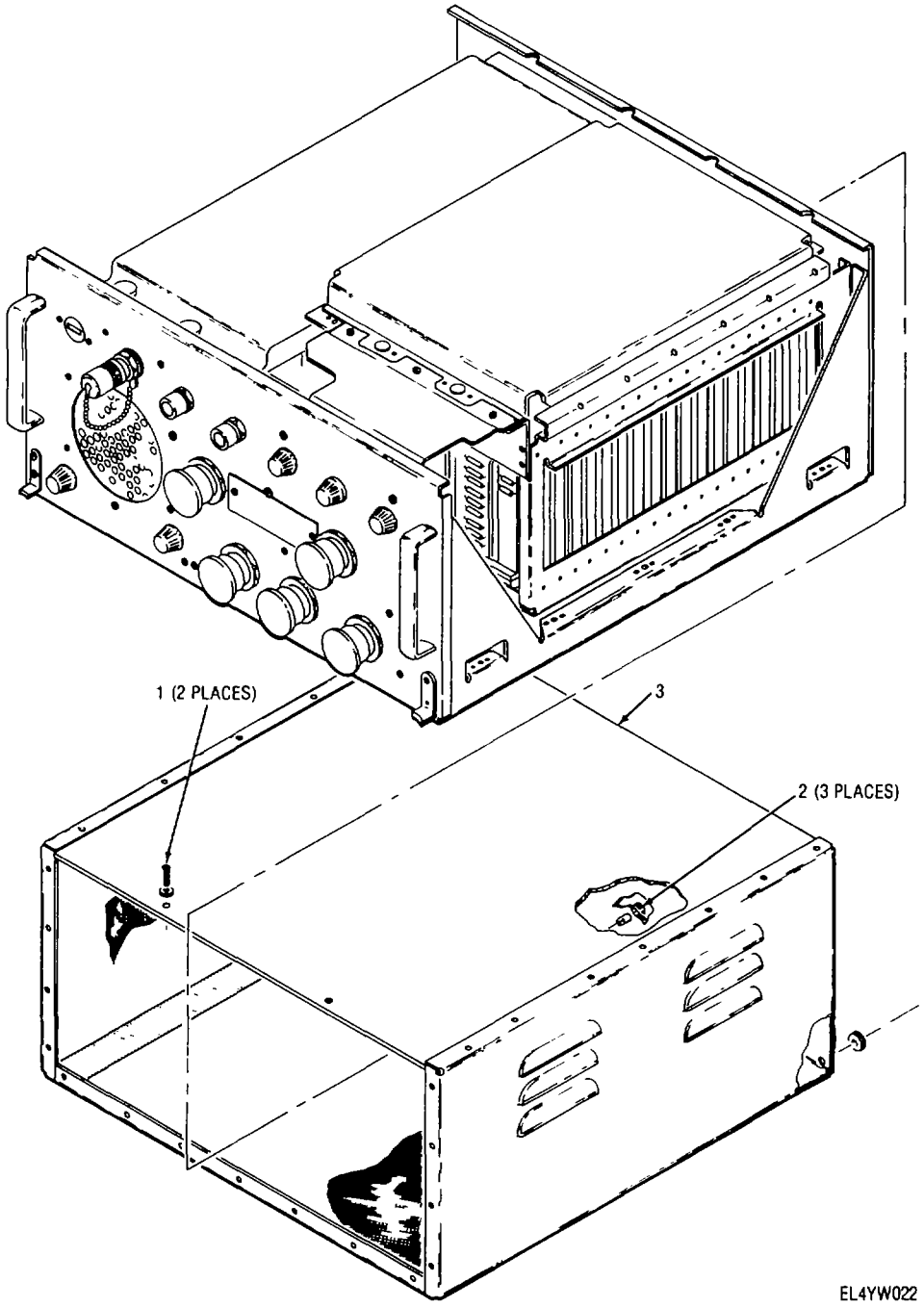


Figure 3-4. Encoder exploded view (sheet 1 of 8).

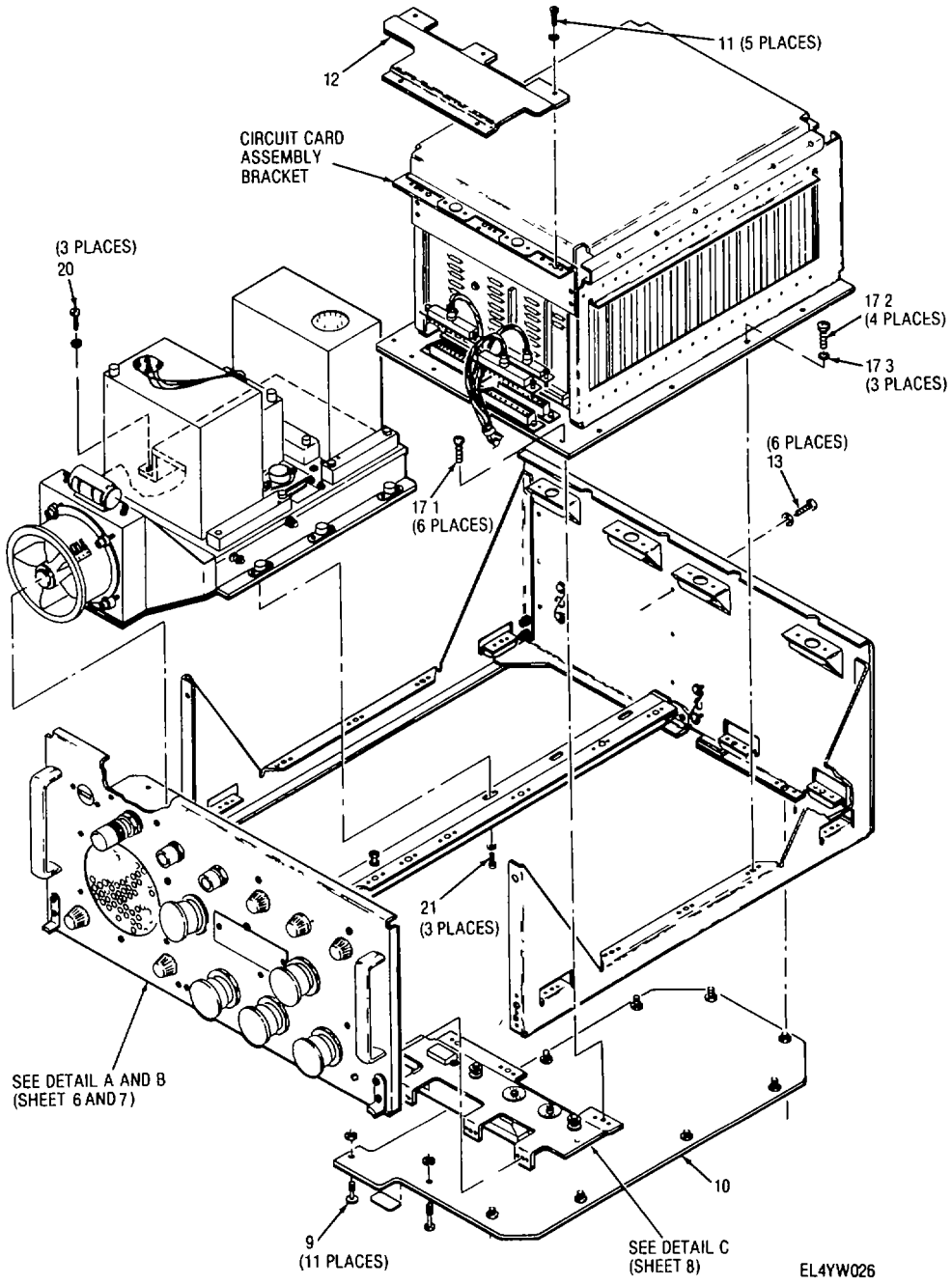


Figure 3-4. Encoder exploded view (sheet 2 of 8).

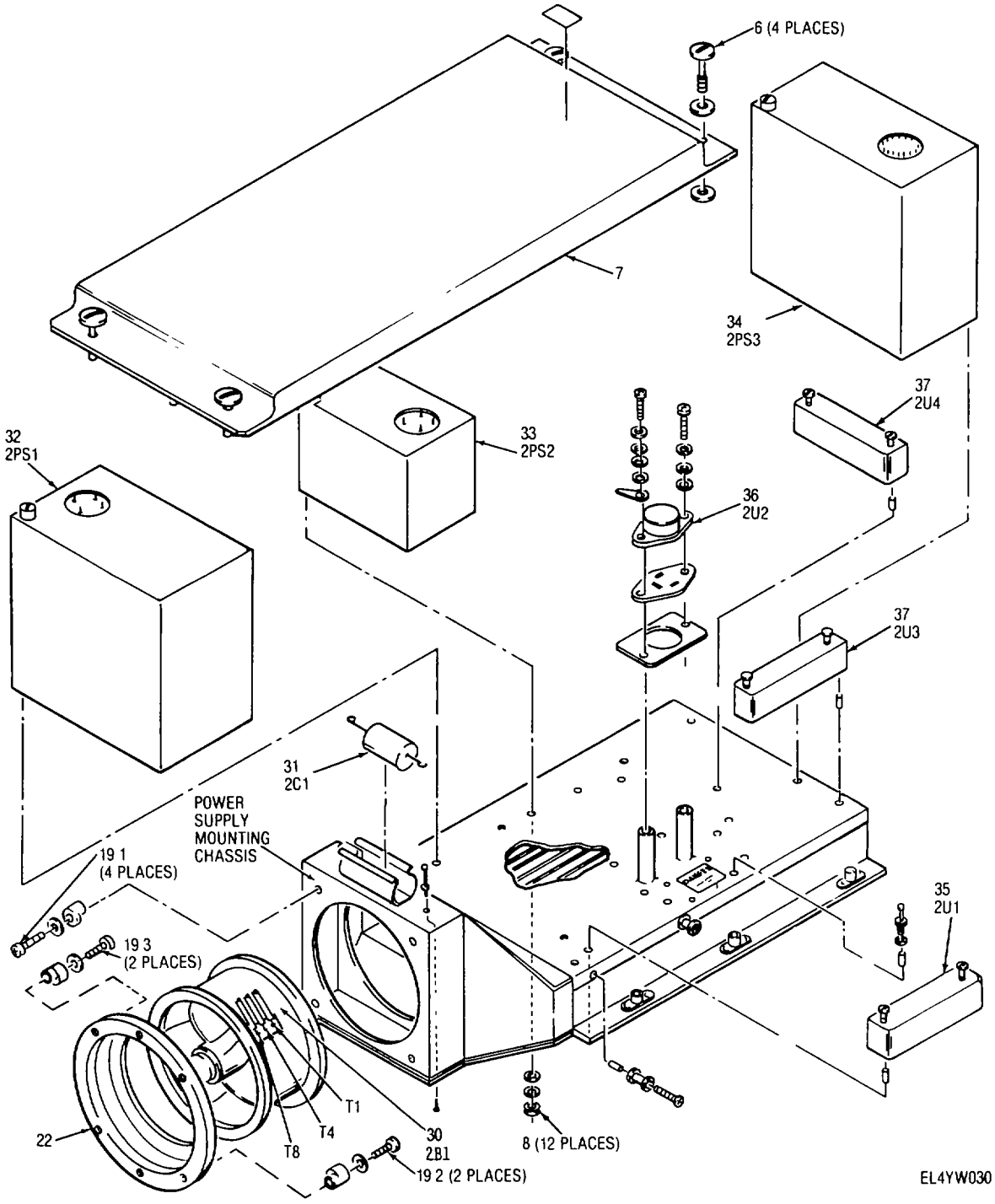


Figure 3-4. Encoder exploded view (sheet 3 of 8).

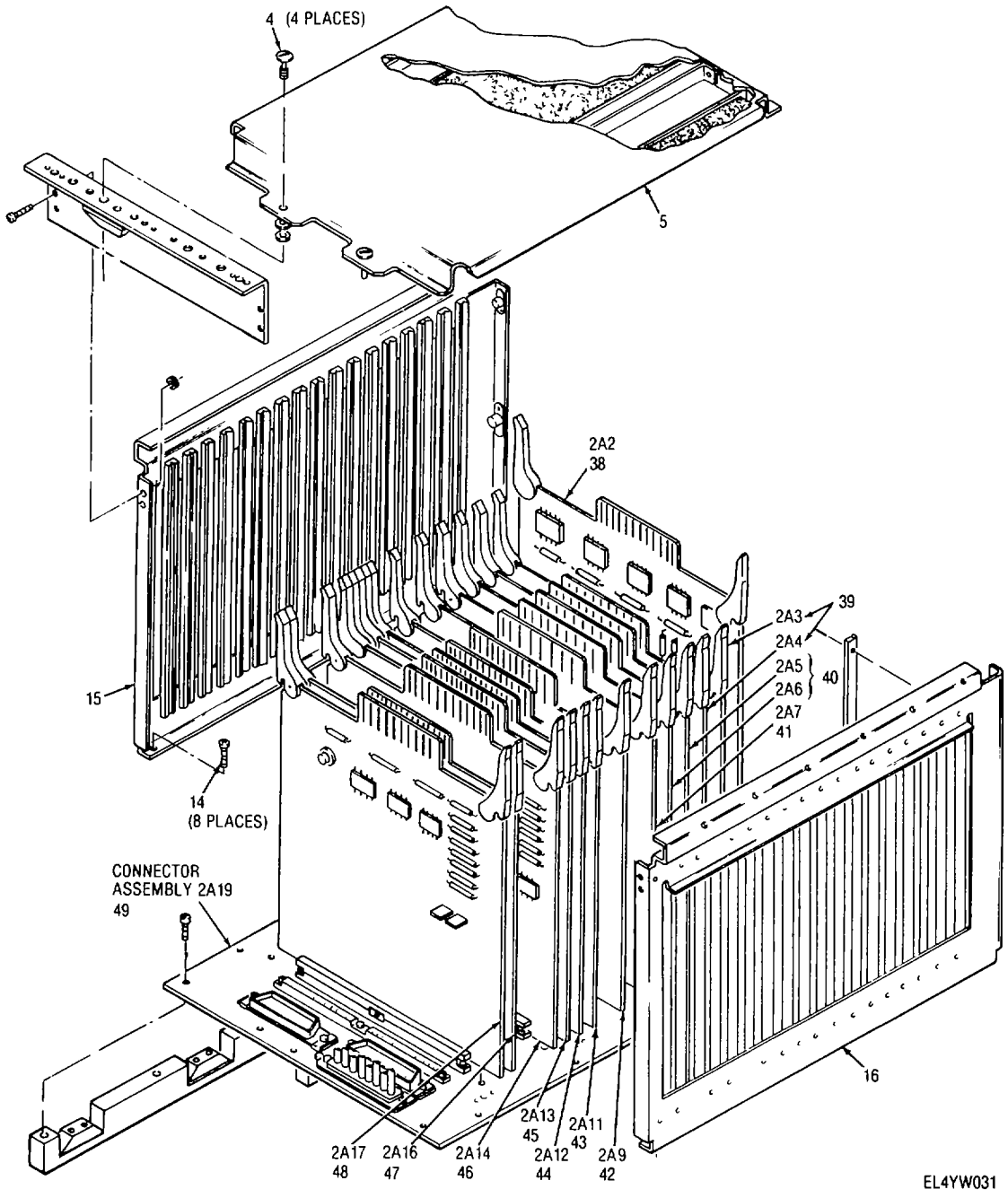


Figure 3-4. Encoder exploded view (sheet 4 of 8).

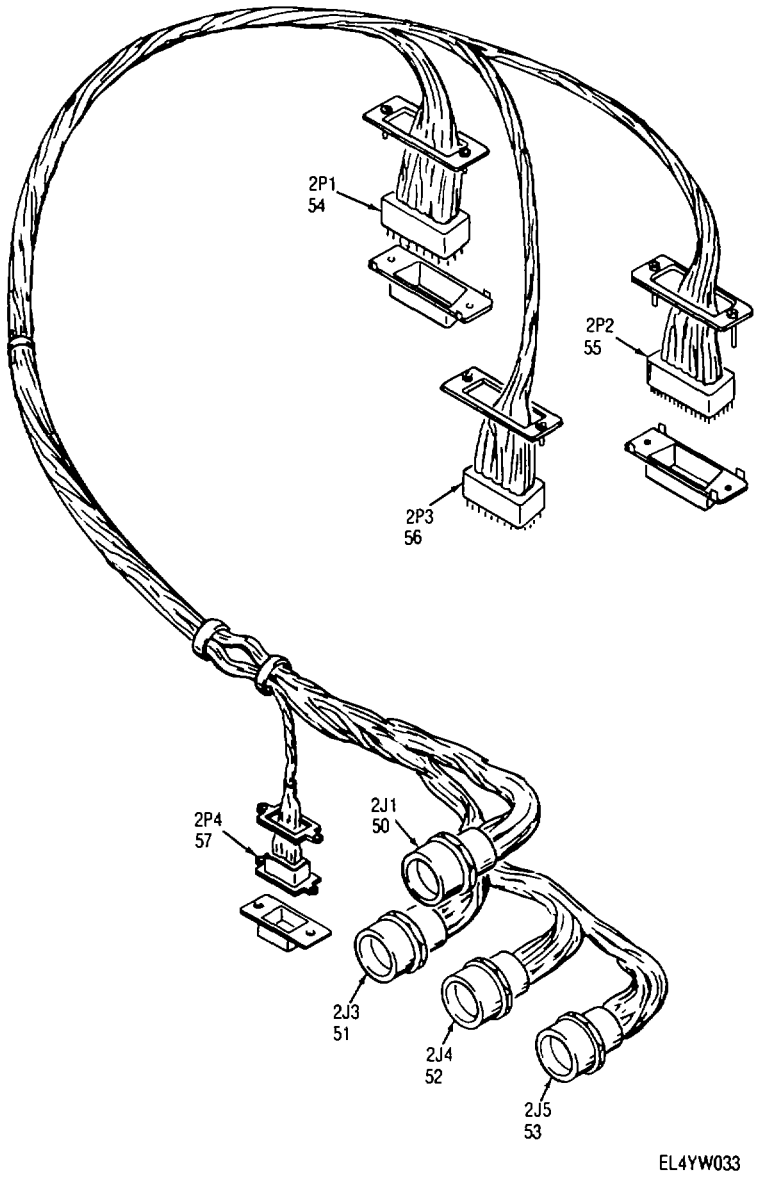


Figure 3-4. Encoder exploded view (sheet 5 of 8).

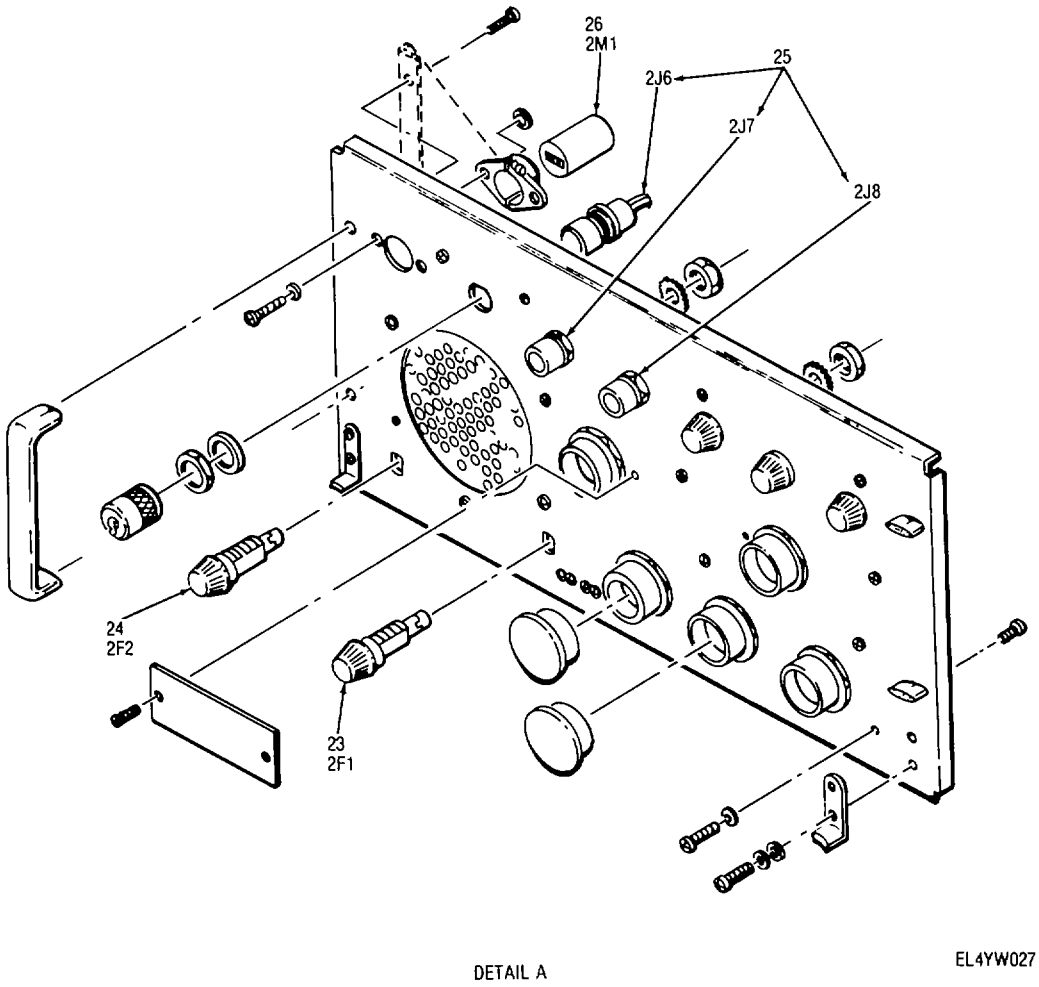


Figure 3-4. Encoder exploded view (sheet 6 of 8).

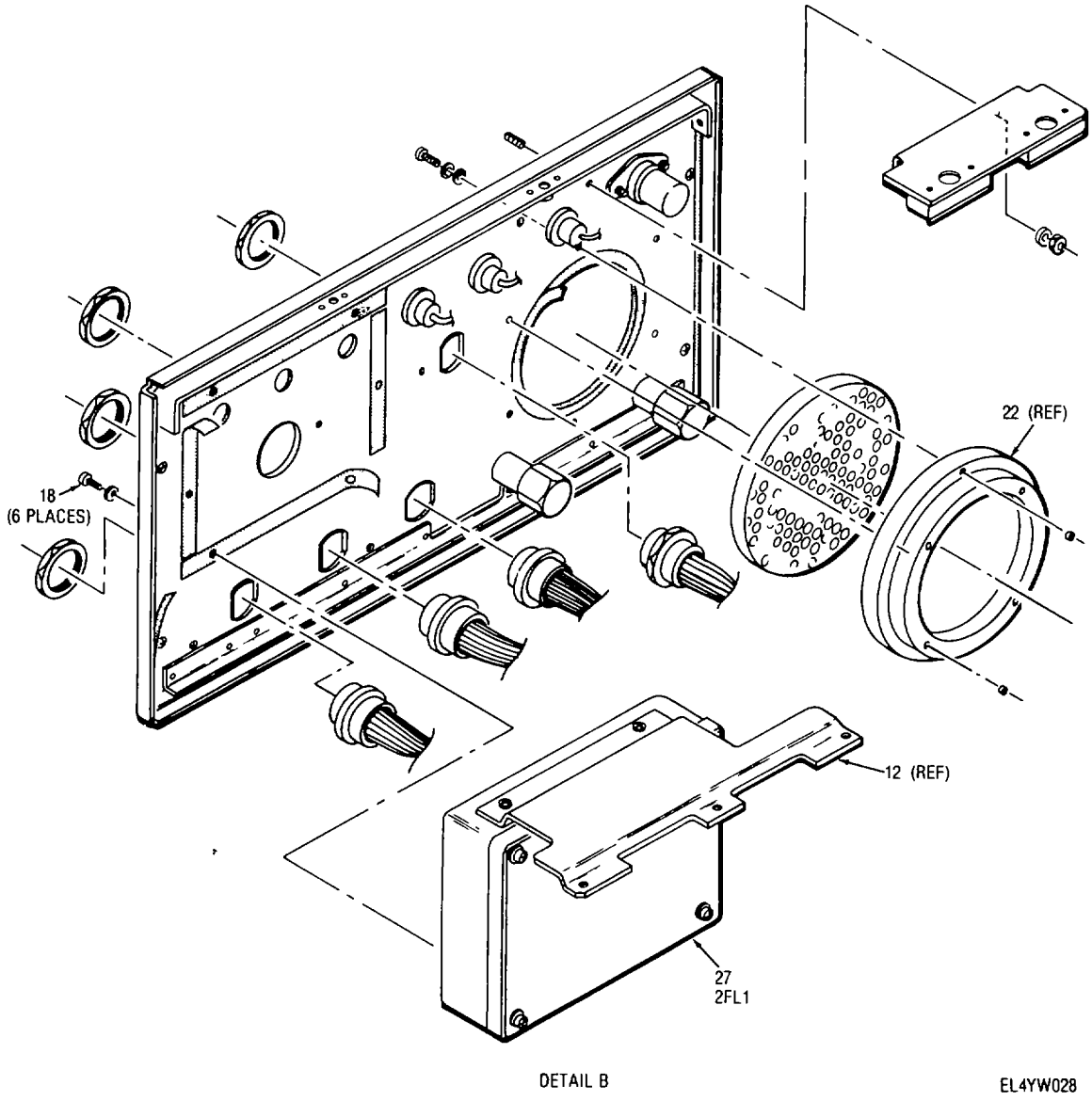


Figure 3-4. Encoder exploded view (sheet 7 of 8).

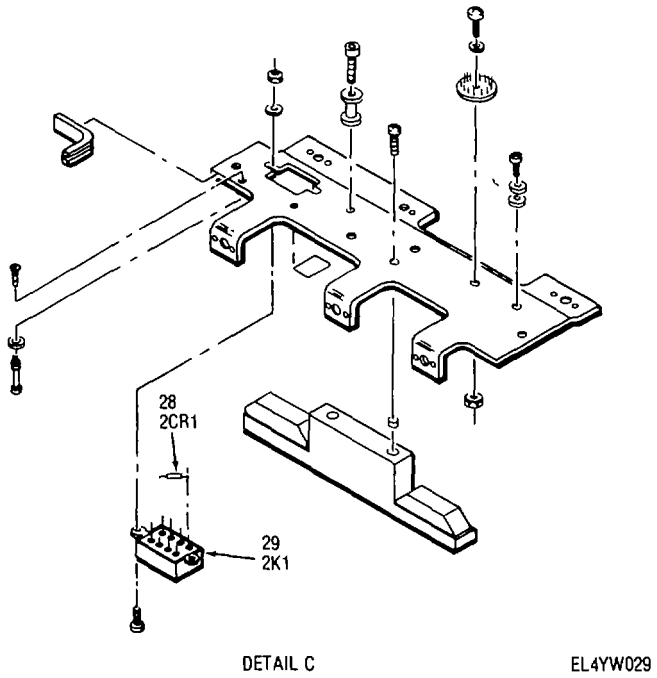


Figure 3-4. Encoder exploded view (sheet 8 of 8).

Legend for figure 3- 4

1 Screw, 8-32 x 1/16; no 8 flat washer (2 places)
2 Quarter-turn fastener (3 places)
3 Outer cover
4 Quarter-turn fastener(4 places)
5 Right inner cover
6 Quarter-turn fastener (4 places)
7 Left inner cover
8 Hex nut, no 10-32, no 10 lockwasher; no 10 flat washer (12 places)
9 Quarter-turn fastener **(11** places)
10 Bottom **inner** cover
11 Screw, 6-32 x 0 375, no 6 flatwasher(5 places)
12 Frontbrace
13 Screw, 6-32 x 0 375, no 6 flat washer (6 places)
14 Screw, 6-32 x 0 375(8 places)
15 Left-hand side plate
16 Right-hand side plate
17 1 Screw, 8-32 x 0 375 (6 places)
17 2 Screw, 6-32 x 0 375(4 places)
17 3 No 6 flatwasher(3 places)
18 Screw, 6-32 x **A, ,** no 6 flat washer (6 places)
19 1 Screw, 4-40 x **0** 500, no 4 flat washer, clamp (4 places)
19 2 Screw, 4-40 x 0 500, no 4 flat washer, clamp (2 places)
19 3 Screw, 4-40 x 0 500, no 4 flatwasher, clamp(2 places)
20 Screw, 8-32 x 0 500, no 8 flat washer (3 places)
21 Screw, 8-32 x 0 500, no 8 flat washer (3 places)
22 Retainer
23 Fuse, 250 V-5 A (2F1)
24 Fuse, 250 V-'X A (2F2)
25 Connector(3 places) (2J6, 2J7, 2J8)
26 Meter, elapsed time (2M1)
27 Filter assembly (2Fll)
28 Diode (2CR1)
29 Relay(2K1)
30 Fan(2B1)
31 Capacitor, 0 27 uf(2Cl1)
32 Power supply, 5 V-1OA (2PS1)
33 Power supply, 5 V-2 5 A (2PS2)
34 Power supply, 12 V-1A (2PS3)
35 Absorber, overvoltage, 2 5-10 V, 10 A **(2U1)**
36 Overvoltage protector, 5 V-6A (2U2)
37 Absorber, overvoltage 5 5-25 V, 1OA (2 places) (2U3, 2U4)
38 Circuit card assembly, AID converter (2A2)
39 Circuit card assembly, FT Accumulator memory (2 places) (2A3, 2A4)
40 Circuit card assembly, MT Accumulator memory (2 places) (2A5, 2A6)
41 Circuit card assembly, video control (2A7)
42 **Circuit** card assembly, video mux (2A9)
43 Circuit card assembly, MPUltlmmng(2All)
44 Circuit card assembly, output buffer (2A12)
45 Circuit card assembly, power fault detector (2A13)
46 Circuit card assembly, output memory (2A14)
47 Circuit card assembly, ADAS control (2A16)
48 Circult card assembly, video interface (2A17)
49 Connector assembly (2A19)
50 Connector(2J1)
51 Connector (2J3)
52 Connector(2J4)
53 Connector (2J5)
54 Connector (2P1)
55 Connector (2P2)
56 Connector (2P3)
57 Connector (2P4)

3-11. Removal and Replacement of Circuit Cards
(fig 3-4)

NOTE

The following procedure is used to remove and replace the plug-in type circuit cards lo-cated in the connector assembly of the encod-er This includes circuit cards 2A2 thru 2A7 (fig. 3-4, sheet 4), 2A9, 2All thru 2A14, 2A16, and 2A17.

a. Removal. Remove circuit card as follows'

(1) Disconnect power to the encoder Place encod-er on a flat surface and in the normal operating posl-tion.

(2) Remove two screws (1, fig 3-4, sheet 1) and washers from top of encoder outer cover (3)

(3) Loosen three quarter-turn fasteners (2) on rear panel of encoder and remove outer cover (3)

(4) Loosen four quarter-turn fasteners (4, sheet 4) on right Inner cover (5), remove right umner cover to gain access to circuit cards

(5) Lift up on card extractors to release selected circuit card from locked position

(6) Grasp selected circuit card firmly and remove by pulling straight up

b. Replacement. Replace circuit card as follows

NOTE

Circuit card positions are numbered from rear panel to front of encoder as Al through A18, respectively

(1) Repeat steps a(1l) through (4) above as neces-sary

(2) Line up circuit card in correct circuit card posl-tlon with component side of circuit card facing toward front of encoder.

(3) With card extractors raised in unlocked posl-tlon (lifted up), apply steady straight-down pressure to align circuit card with circuit card connector

(4) Press down on card extractors until circuit card is locked in position and properly seated m circuit card connector

(5) Replace right inner cover (5, fig 3-4, sheet 4) over circuit cards. Secure cover by tightening four quarter-turn fasteners (4)

(6) Replace outer cover (3, sheet 1) over encoder Secure cover by replacing two screws (1) and washers in top of outer cover and tightening three quarter-turn fasteners (2) on rear panel.

3-12. Removal and Replacement of Power Supply 2PS1
(fig. 3-4)

a. Removal. Remove power supply 2PS1 (fig. 3-4, sheet 3) as follows'

(1) Disconnect power to encoder. Place encoder on a flat surface and in the normal operating position

(2) Remove two screws (1, fig. 3-4, sheet 1) and washers from top of encoder outer cover (3)

(3) Loosen three quarter-turn fasteners (2) on rear panel of encoder and remove outer cover (3).

(4) Loosen four quarter-turn fasteners (6, sheet 3) on left Inner cover (7) Remove left Inner cover to gain access to power supply 2PS1.

(5) Locate power supply 2PS1 and tag wires con-nected to its four terminals (10 wires).

(6) Unsolder wires tagged in step (5) from power supply 2PS1 terminals and place carefully aside

(7) Place encoder on its right side to gain access to power supply 2PS1 mounting hardware

CAUTION

Hold power supply 2PS1 securely to prevent damage to adjacent hardware and circuit cards while performing steps (8) and (9)

(8) Remove four nuts (8) and eight washers secur-ing power supply 2PS1 to bottom of power supply mounting chassis

(9) Remove power supply 2PS1 from mounting surface of chassis by pulling straight out

b. Replacement Replace power supply 2PS1 as fol-lows:

(1) Repeat steps a(1l) through (4) above as neces-sary.

(2) Apply a thin, even coating of silicone heat sink compound (Dow Corning 340) to base of power supply 2PS1 and to chassis mounting surface for power sup-ply 2PS1.

(3) Position power supply 2PS1 on chassis mount-ing surface. Install and tighten four nuts (8, fig 3-4, sheet 3) and eight washers to secure power supply.

(4) Place encoder in upright position.

(5) Reconnect wires to power supply 2PS1 termi-nals (refer to fig FO-4 and table 3-8 for applicable wirng information). Remove tags.

(6) Replace left inner cover (7) over power supply 2PS1 Secure over by tightening four quarter-turn fasteners (6).

(7) Replace outer cover (3, sheet 1) on encoder. Se-cure cover by replacing two screws (1) and washers in top of cover (3) and tightening three quarter-turn fasteners (2) on rear panel

3-13. Removal and Replacement of Power Supply 2PS2
(fig 3-4)

a. Removal. Remove power supply 2PS2 (fig. 3-4, sheet 3) as follows

(1) Disconnect power to the encoder. Place encod-er on a flat surface and in the normal operating posi-tion

(2) Remove two screws (1, fig. 3-4, sheet 1) and washers from top of encoder outer cover (3)

(3) Loosen three quarter-turn fasteners (2) on rear

panel of encoder and remove outer cover (3).

(4) Loosen four quarter-turn fasteners (6, sheet 3) on left inner cover (7) Remove left inner cover to gain access to power supply 2PS2

(5) Tag wires connected to the four terminals (six wires) on power supply 2PS2

(6) Unsolder wires tagged in step (5) from power supply 2PS2 terminals and place carefully aside

(7) Place encoder on right-hand side to gain access to power supply 2PS2 mounting hardware.

CAUTION

Hold power supply 2PS2 securely when removing mounting hardware to prevent damage to adjacent hardware and circuit cards

(8) Remove four nuts (8) and eight washers secur-ing power supply 2PS2 to bottom of power supply mounting chassis

(9) Remove power supply 2PS2 from chassis

b. Replacement Replace power supply 2PS2 as fol-lows:

(1) Repeat steps a(l) through (4) above as neces-sary

(2) Apply a thin, even layer of silicone heat sink compound (Dow Corning 340) to base of power supply 2PS2 and to chassis mounting surface for power sup-ply 2PS2

(3) Position power supply 2PS2 on mounting sur-face of chassis Install and tighten four nuts (8, fig 3-4, sheet 3) and eight washers to secure power sup-ply

(4) Place encoder in upright position

(5) Connect wires to power supply 2PS2 terminals (refer to fig. FO-4 and table 3-8 for applicable wlrng information). Remove tags

(6) Replace left inner cover (7) power supply 2PS2 Secure cover by tlghtemng four quarter-turn fasteners (6)

(7) Replace outer cover (3, sheet 1) on encoder Secure cover by replacing two screws (1) and washers m top of cover (3) and tightening three quarter-turn fasteners (2) on rear panel

3-14. Removal and Replacement of Power Supply 2PS3 (fig. 3-4)

a. Removal Remove power supply 2PS3 (fig 3-4, sheet 3) as follows

(1) Disconnect power to the encoder Place encod-er on a flat surface and in the normal operating position

(2) Remove two screws (1, fig 3-4, sheet 1) and washers from top of encoder outer cover (3)

(3) Loosen three quarter-turn fasteners (2) on rear panel of encoder and remove outer cover (3).

(4) Loosen four quarter-turn fasteners (6, sheet 3) on left inner cover (7). Remove left inner cover to gain access to power supply 2PS3

(5) Locate power supply 2PS3 and tag wires con-nected to its eight terminals (five wires)

(6) Unsolder wires tagged in step (5) from power supply 2PS3 terminals and place carefully aside

(7) Place encoder on right-hand side to gain access to power supply 2PS3 mounting hardware

CAUTION

Hold power supply 2PS3 securely when removing mounting hardware to prevent damage to adjacent hardware and circuit cards

(8) Remove four nuts (8) and eight washers secur-ing power supply 2PS3 to bottom of power supply mounting chassis.

(9) Remove power supply from mounting surface of chassis by pulling straight out

b. Replacement Replace power supply 2PS3 as fol-lows

(1) Repeat steps a(l) through (4) above as neces-sary.

(2) Apply a thin, even layer of silicone heat sink compound (Dow Corning 340) to base of power supply 2PS3 and to chassis mounting surface **for** power sup-ply 2PS3.

(3) Position power supply 2PS3 on mounting sur-face of chassis. Install and tighten four nuts (8, fig 3-4, sheet 3) and eight washers to secure power sup-ply

(4) Place encoder in upright position

(5) Reconnect wires tagged previously to power supply 2PS3 terminals (refer to fig FO-4 and table 3-8 for applicable wiring information) Remove tags.

(6) Replace left Inner cover (7) over power supply 2PS3. Secure cover by tightening four quarter-turn fasteners (6).

(7) Replace outer cover (3, sheet 1) on encoder Se-cure cover by replacing two screws (1) and washers in top of cover (3) and tightening three quarter-turn fasteners (2) on rear panel

3-15. Removal and Replacement of Connector Assembly 2A19 (fig. 3-4)

a. *Removal.* Remove connector assembly 2A19 (fig 3-4, sheet 4) as follows.

(1) Disconnect power to the encoder Place encod-er on flat surface and in the normal operating position

(2) Remove two screws (1, fig. 3-4, sheet 1) and washers from top of encoder outer cover (3).

(3) Loosen three quarter-turn fasteners (2) on rear panel of encoder and remove outer cover (3)

(4) Loosen four quarter-turn fasteners (4, sheet 4) on right inner cover (5) Remove right inner cover to gain access to circuit cards and connector assembly 2A19

(5) Release circuit card 2A2 from locked position by lifting up on card extractors

(6) Grasp circuit card 2A2 firmly and remove by

pulling straight up

(7) Repeat steps (5) and (6) for the remaining cir-cuit cards

(8) Place encoder on left-hand side to gain access to bottom inner cover (10, sheet).

(9) Loosen 11 quarter-turn fasteners (9) on bottom inner cover Remove bottom Inner cover

(10) Place encoder in upright position.

(11) Remove five screws (11, sheet 2) and washers securing front brace (12) between filter 2FL1 and cir-cult card assembly bracket. Remove front brace.

(12) Remove six screws (13, sheet 2) and washers securing left and righthand side plates (15 and 16) to rear panel of encoder.

(13) Remove eight screws (14, sheet 4) securing left (15) and right-hand side plates (16) to connector assembly 2A19 Remove left and right-hand side plates.

(14) Loosen six screws securing internal connectors 2P1 thru 2P3 (sheet 5) to connectors J1 thru J3 of connector assembly 2A19.

(15) Disconnect internal connectors 2P1 thru 2P3 and set aside carefully

(16) Remove six screws (17.1, sheet 2), four screws (17 2), and (17 3) three washers securing connector as-sembly 2A19 to mounting surface on bottom of chassis.

(17) Remove connector assembly 2A19, being careful to clear rear panel.

(18) Replace bottom inner cover to protect wire wrap pins

b. Replacement Replace connector assembly 2A19 as follows.

(1) Perform steps a(1l**)** through (4) above as neces-sary Remove bottom Inner cover from connector as-sembly.

(2) Position replacement connector assembly on mounting surface on bottom of chassis (fig 3-4, sheet 2**)**

NOTE

Use three washers (17 3) in step (3) below with three screws (17.2) located at front of connector assembly 2A19 In steps (3) and (6) through (8) below, thread screws m to holes finger tight They will be tightened later

(3) Secure connector assembly 2A19 to chassis mounting surface with six screws (17 1, sheet 2), four screws (17 2), and three washers (17 3).

(4) Connect internal connectors 2P1 thru 2P3 (fig 3-4, sheet 5) to connectors J1 thru J3 (fig. 3-4, sheet 7) of connector assembly 2A19

(5) Secure internal connectors 2P1 thru 2P3 to connector assembly 2A19 with six screws.

(6) Secure left-hand and right-hand side plates (15 and 16) to connector assembly 2A19 with eight screws (14).

(7) Secure left-hand and right-hand side plates to rear panel of encoder with six screws (13, sheet 2) and washers.

(8) Secure front brace (12) to filter 2Fll and cir-cuit card assembly bracket with five screws (11) and washers

(9) Place encoder on left-hand side

(10) Replace bottom inner cover (10) over bottom of connector assembly 2A19 Secure cover by tightening 11 quarter-turn fasteners (9).

(11) Place encoder in upright position

NOTE

Circuit card positions are numbered from rear panel to front of encoder as Al thru A18, respectively

(12) Line up circuit card 2A2 (sheet 4) in correct circuit card position with component side of circuit card facing toward front of encoder

(13) With card extractors raised in unlocked posi-tion (lifted up) apply steady straight down pressure to align circuit card in circuit card connector.

(14) Press down on card extractors until circuit card **is** locked in position and properly seated m circuit card connector

(15) Repeat steps (12) through (14) for **circuit** cards, 2A9 and 2A17

(16) With left-hand and right-hand side plates (15 and 16) and front brace (12, sheet 2) loosely held together, align parts and alternately tighten each screw. As screws are being tightened, realign parts (as neces-sary) to allow free, smooth removal and replacement of circuit cards When properly aligned, tighten all screws installed **in** steps (3) and (6) through (8)

(17) Repeat steps (12) through (14) for remaining circuit cards

(18) Replace right Inner cover (5) over circuit cards Secure over by tightening four quarter-turn fasteners (4)

(19) Replace outer cover (3, sheet 1) over encoder Secure cover by tightening three quarter-turn fasteners (2) on rear panel and replacing two screws (1) in top cover.

3-16. Removal and Replacement of Filter 2FL1

(fig. 3-4)

a. Removal. Remove filter 2FL1 (fig 3-4, sheet 7 and table 3-9) as follows.

(1) Disconnect power to the encoder. Place encod-er on a flat surface and **in** the normal operating posi-tion

(2) Remove two screws (1, sheet 1) and washers from top of encoder outer cover (3).

(3) Loosen three quarter-turn fasteners (2) on rear panel of encoder and remove outer cover (3)

(4) Remove five screws (11, sheet 2) and washers

securing front brace (12) between filter 2FL1 and cir-cuit card assembly bracket Remove front brace CAUTION Hold filter 2FL1 securely to prevent damage to adjacent hardware and circuit cards while performing steps (5) and (6)

(5) Remove six screws (18, sheet 7) and washers securing filter 2FL1 to front panel of encoder

(6) Loosen filter 2FL1 by backing it out until it clears front panel.

(7) Loosen two screws securing connector 2P4 (sheet 5) to filter 2FL1 connector J1

(8) Disconnect connector 2P4 from filter 2FL1 connector J1 and set aside carefully

(9) Remove filter 2FL1 by backing it out until it clears front panel and then lifting straight up

b. Replacement Replace filter 2FL1 (fig 3-4, sheet 7) as follows'

(1) Repeat steps a(1l) thru (3) above as necessary

(2) Position replacement filter on front panel

(3) Reconnect connector 2P4 (sheet 5) to filter 2FL1 connector J1

(4) Secure connector 2P4 to filter 2FL1 connector J1 with two screws.

(5) Secure replacement filter 2FL1 to front panel with six screws (18) and washers

(6) Secure front brace (12, sheet 2) to filter 2FL1 and circuit card assembly bracket with five screws (11) and washers

(7) Replace outer cover (3, sheet 1) over encoder.

Secure cover by replacing two screws (1) and washers in top of cover (3) and tightening three quarter-turn fasteners (2) on rear panel

3-17. Removal and Replacement of Fan 2B1

(fig 3-4)

a. *Removal* Remove fan 2B1 (fig. 3-4, sheet 3) as follows

(1) Disconnect power to the encoder. Place encod-er on a flat surface and in the normal operating posi-tion

(2) Remove two screws (1, sheet 1) and washers from top of encoder outer cover (3)

(3) Loosen three quarter-turn fasteners (2) on rear panel of encoder and remove outer cover (3)

(4) Loosen four quarter-turn fasteners (6, sheet 3) on left inner cover (7) Remove left inner cover to gain access to fan 2B1(30)

(5) Locate fan 2B1 and tag three wires connected to terminals T1, T4, and T8

(6) Loosen three screws securing wires tagged m step (5). Disconnect wires from fan 2B1 terminals and place carefully aside

(7) Place encoder on its right side to gain access to fan 2B1 mounting hardware.

(8) Remove four screws (19 1), washers, and clamps securing fan 2B1 to power supply mounting chassis.

CAUTION

Hold power supply mounting chassis securely since it is heavy and may damage adjacent hardware if dropped

(9) Loosen, but do not remove, three screws (20, sheet 2) on top and three screws (21) on bottom of power supply mounting chassis

(10)Slide power supply mounting chassis toward rear panel as far as slotted holes will allow Tighten top and bottom screws loosened m step (9)

(11)Remove two screws (19 2, sheet 3), washers, and clamps securing bottom of fan 2B1 to retainer (22)

(12)Loosen, but do not remove, two screws (19.3) and clamps securing top of fan 2B1 to retainer Care-fully slide fan out through bottom of encoder chassis

b. Replacement Replace fan 2B1 (fig. 3-4, sheet 3) as follows.

(1) Repeat steps a(1l**)** through (4) above as neces-sary

(2) Position replacement fan on retainer (22) so that air flow indicator arrow on fan 2B1 (30) is point-ing away from front panel.

(3) Secure fan 2B1 to retainer with four screws (19 2 and 19 3), washers, and clamps.

CAUTION

Hold power supply mounting chassis securely since it is heavy and may damage adjacent hardware if dropped.

(4) Loosen, but do not remove, three screws (20, sheet 2) on top and three screws (21) on bottom of power supply mounting chassis

(5) Slide power supply mounting chassis as far as possible toward front panel to mate with fan 2B1. Finger tighten top and bottom screws loosened in step (4)

(6) Secure fan 2B1 to power supply mounting chassis (sheet 3) with four screws (19 1), washers, and clamps

(7) Secure power supply mounting chassis with top and bottom screws (20 and 21, sheet 2)

(8) Reconnect previously tagged wires to three terminals (T1, T4, and T8) of fan 2B1 (refer to fig. FO-4 and table 3-8) Tighten three screws to secure wires to terminals Remove tags

(9) Place encoder in the upright position

(10)Replace left inner cover (7, sheet 3) over fan 2B1 Secure cover by tightening four quarter-turn fasteners (6)

(11)Replace outer cover (3, sheet 1) over encoder.

Secure cover by replacing two screws (1) and washers in top of cover (3) and tightening three quarter-turn fasteners (2) on rear panel.

3-18. Removal and Replacement of Connectors

Instructions for removal and replacement of connectors are provided in the following subparagraphs No special tools are required Refer to figures 3-4 and 3-5 for parts location details

a. Connectors 2J1, 2J3, 2J4, 2J5 (fig 3-4, sheet 5), and 3J1 (fig. 3-5)

NOTE

Steps (1) and (2) are applicable to repair of connectors 2J1, 2J3, 2J4, and 2J5 only

(1) Perform steps (1) through (4) of paragraph 3-1 *a* as necessary

(2) Detach filter assembly 2FL1 (sheet 7) from front panel assembly as follows

(a) Remove five screws (11, sheet 2) and washers and remove front brace (12)

(b) Loosen two attached screws on connector 2P4 and remove connector.

© Remove six screws (18, sheet 7) and washers holding filter assembly 2FL1 to front panel assembly

(3) Remove nut (supplied with connector) and detach connector from its mounting position

(4) Unscrew threaded rear section of connector and slide insert back to expose contacts

(5) Carefully unsolder and tag connector wires

NOTE

Be sure to thread wires through rubber insert and threaded back section of connector be fore soldering After soldering is completed, slide rubber insert back in place and tighten rear section of connector

(6) Solder tagged connector wires to matching contacts of new connector. Remove tags

(7) Mount assembled connector m place and secure with nut supplied

(8) Secure filter assembly 2FL1 to front panel as-sembly using six screws (18) and washers

(9) Secure connector 2P4 with two attached screws.

(10) Install front brace (12, sheet 2) between circuit card assembly bracket and filter assembly 2FL1 using five screws (11) and washers

b. Connectors 2P1, 2P2, and 2P3 and 2P4 (fig 3-4, sheet 5)

(1) Perform steps (1) through (4) of paragraph 3- 1a as necessary

(2) Remove five screws (11, sheet 2) and washers and remove front brace (12)

(3) Loosen two captive screws (supplied with connector) and unplug connector from receptacle.

(4) Carefully unsolder wires from defective connector and tag each wire

(5) Solder connector wires to contacts of new connector. Remove tags

(6) Insert assembled connector into corresponding receptacle and tighten two captive screws

(7) Install front brace (12) between circuit card assembly bracket and filter assembly 2F1 using five screws (11) and washers

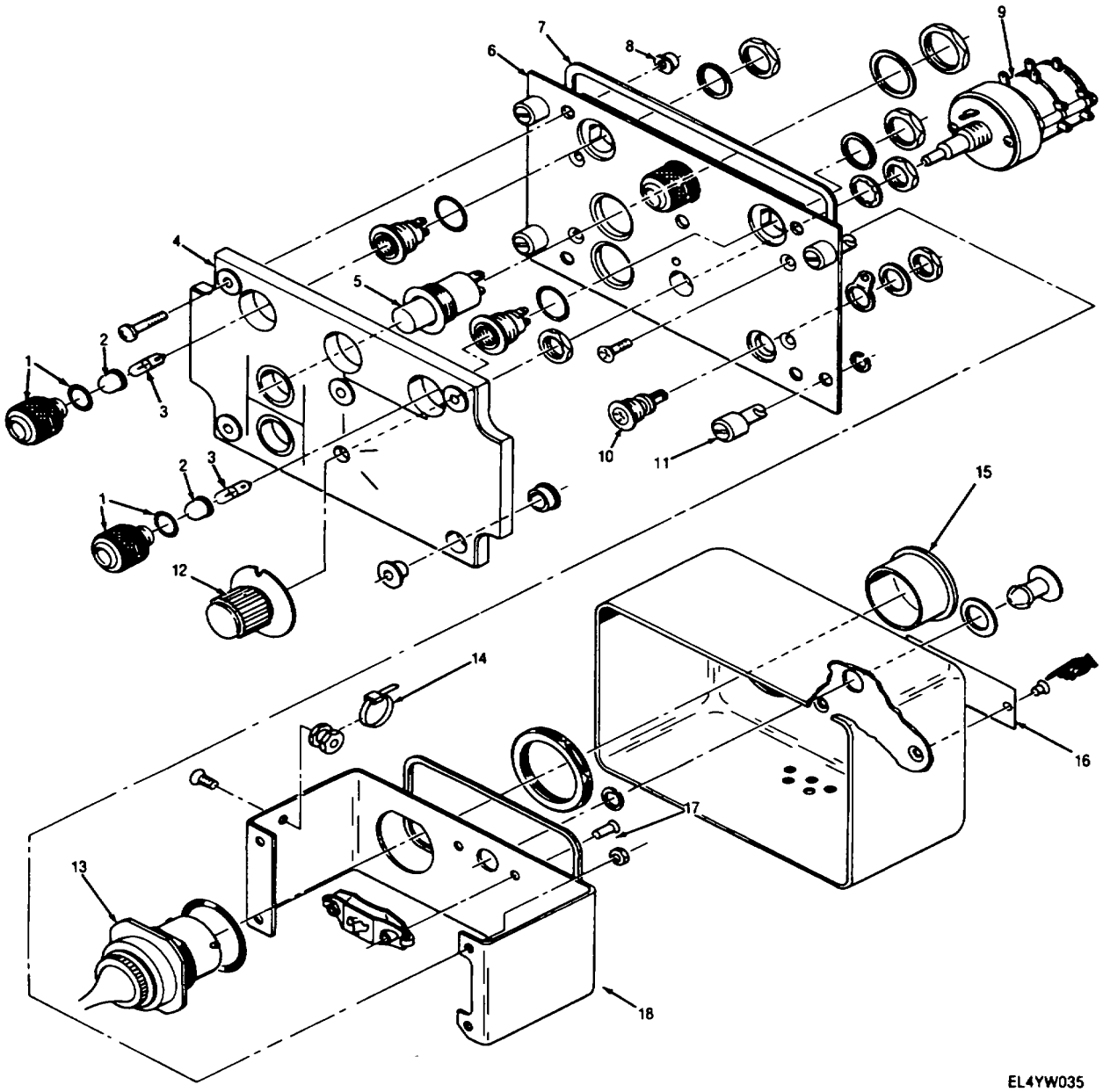


Figure 3-5. Data link control exploded view

Legend for figure 3-5:

1 Housing indicator light (2 places)
2 Lens indicator light (2 places)
3 Lamp incandescent **(2** places)
4 Panel indicator light mounting
5 Switch
6 Plate mounting
7 Shield, gasket
8 Nut self-locking
9 Switch rotar
10 Connector, receptacle
11 Stud assembly, turnlock
12 Knob
13 Connector, receptacle
14 Strap tiedown
15 Cap, protective
16 Plate identification
17 Shield, gasket
18 Bracket

3-19. Removal and Replacement of Chassis-Mounted Parts and Panel Mounted Parts

(fig. 3-4 and 3-5)

There are no special instructions for the removal and replacement of chassis-mounted parts No special tools are required. When replacing parts, use standard shop methods Refer to figure 3-4 when replacing parts on the encoder and to figure 3-5 and table 3-10 when replacing parts on the data link control.

a. Make sure replacement resistors, capacitors, fuses, lamps, etc are of the same value and type of the one replaced.

b. Use epoxy coating sparingly on those hardware items requiring epoxy coating

c. Tag wires for identification on wired components.

d. Make sure all hardware items such as washers, lockwashers, setscrews, etc are installed when replacing knobs, controls, switches, etc

3-20. Repair of Electrical Filter Assembly 2FL1

(fig 3-6)

Repair of electrical filter assembly 2FL1 is performed by making continuity checks and replacing defective parts Refer to figure 3-6 for the location of filter parts and the schematic A wire hst for the filter assembly is shown on table 3-9

3-21. Adjustments

(fig 3-7)

WARNING

During adjustment, dangerous potentials up to 115 V ac are applied to exposed terminals and wiring In the encoder chassis Exercise extreme caution when working inside this chassis throughout the rest of thus procedure.

The following paragraphs contain information for adjusting the encoder dc power supplies (2PS1, 2PS2, 2PS3) and associated overvoltage protectors (2U1, 2U3, 2U4). Adjustments are required when any of the power supplies or overvoltage protectors are replaced or when faults are indicated during the functional test-
ng Refer to figure 3-7 for location of all power sup-
ply adjustments and test points

a Test Equipment Required. The following test equipment is required for performance of the adjust-ment procedures.

Test equipment.	*Common name*
digital Voltmeter. ANIGSM-64B	Digital voltmeter (DVM)
Test Set, Electronic Systems TS-3796/UKM-4	Control interface unit

b. Power Supply Output Voltage Adjustments.

(1) Perform steps (1) through (4) of paragraph 3-12a to gain access to the encoder power supplies.

(2) Connect the equipment as shown in figure 3-1.

(3) Prior to adjusting the encoder power supplies, refer to figure 3-7 for the location of the overvoltage protectors (2U1, 2U3, 2U4). Set all overvoltage protector ADJ screws to their maximum clockwise (cw) rota- \partion.

(4) Connect the digital voltmeter (DVM) between terminals 3 and 4 (gnd) on power supply 2PS1 (fig. 3-7).

(5) Turn the equipment on by setting the equip-ment controls as follows.

(a) Set the control interface unit POWER ON/OFF switch to ON and the MODE SELECT switch to UNIT TEST ENC.

(b) Set the data link control POWER switch to STBY.

(6) Adjust power supply 2PS1 ADJ POT for + 5 + 0. 1 volts

(7) Set the data link control POWER switch to OFF

(8) Connect the DVM between terminals 4 and 3 (gnd) on power supply 2PS2.

(9) Set the data link control POWER switch to STBY.

(10) Adjust power supply 2PS2 ADJ POT for -5 + 1 volts.

(11) Set the data link control POWER switch to OFF

(12) Connect the DVM between terminals 3 and 4 (gnd) on power supply 2PS3.

(13) Set the data link control POWER switch to STBY.

(14) Adjust power supply 2PS3 ADJ POT for + 12 + 0.1 volts Connect DVM positive lead to 2PS3 pin 5. Check for - 12 _ 0.1 volts.

(15) Set the data link control POWER switch to OFF.

c. Overvoltage Protector/Adjustments.

NOTE

The DVM connected in the following steps will be used to indicate when the overvoltage protectors have been activated.

(1) Connect the DVM between terminals 3 and 4 (gnd) of power supply 2PS1.

(2) Set the data link control POWER switch to STBY.

(3) Slowly adjust overvoltage protector 2U1 ADJ potentiometer (fig. 3-7) counterclockwise (ccw) until the + 5 volt supply short-circuits.

(4) Set the data link control POWER switch to OFF and adjust 2U1 ADJ potentiometer clockwise six complete turns. Overvoltage protector 2U1 is now set to trip at + 6 8 volts.

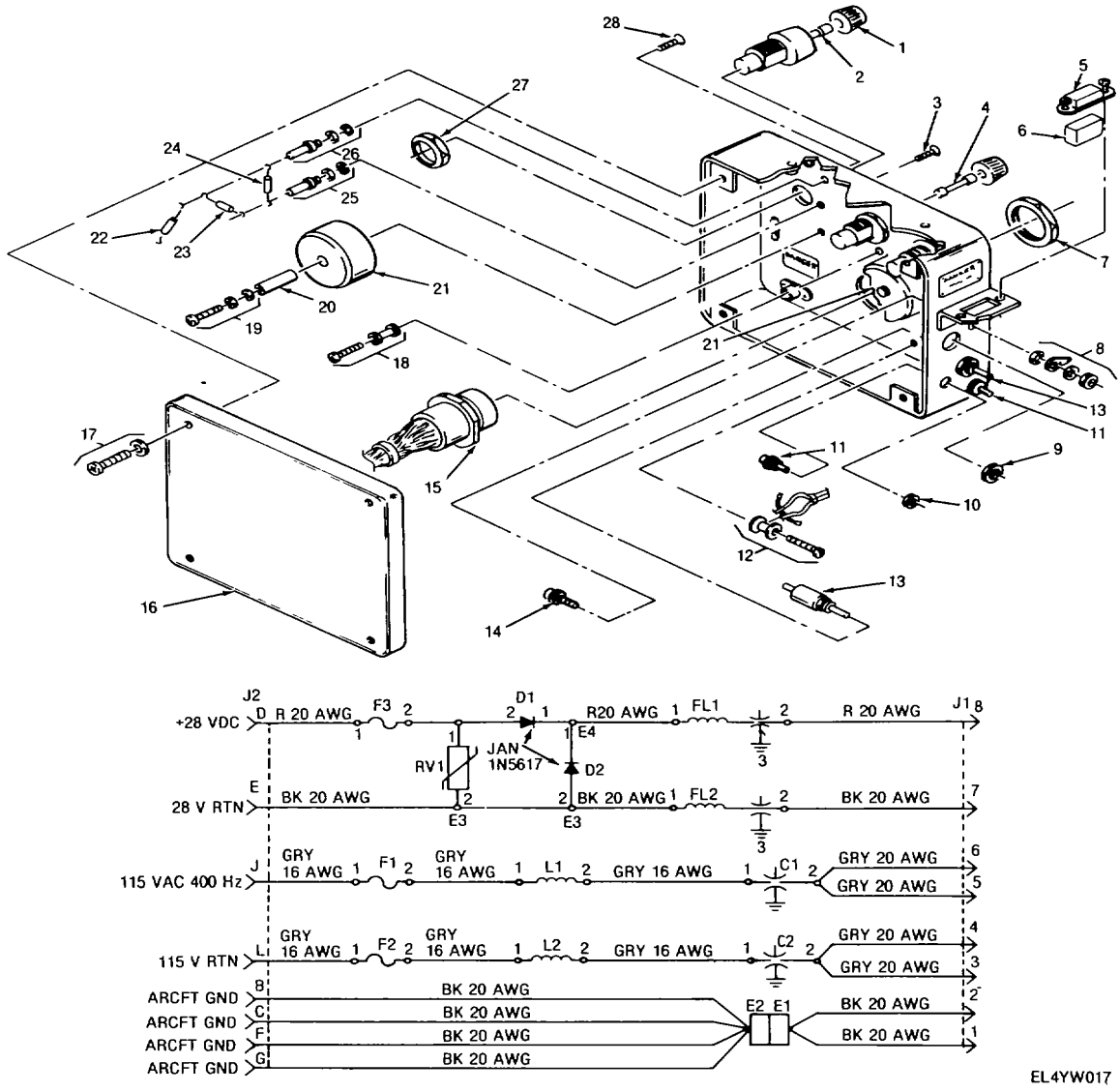


Figure 3-6. Electrical Filter assembly 2FL1 parts location and schematic diagram

Legend for figure 3-6

1 Fuseholder(3 places)
2 Fuse(F3)
3 Screw
4 Fuse (F2)
5 Connector (J ***1)***
6 Sleeving
7 Nut, **locking** *(P0* **J2)**
8 Nut, washer, terminal, washer
9 Nut(PIO Cl)
10 **Nut(PIOFL1)**
11 Filter (2 places) (FL1, FL2)
12 Clamp, screw
13 Capacitor(2 places)(Cl, C2)
14 Screw
15 Connector(J2)
16 Cover
17 Screw, washer
18 Screw, clamp
19 Screw, washer, washer
20 Post
21 Reactor, (2 places) (L1, L2)
22 Resistor, voltage sensitive (RV1)
23 Dlode(D1)
24 Diode(D2)
25 Terminal, washer, washer (E4)**3-29**
26 Terminal, washer, washer (E3)
27 Nut(PIO iteml)
28 Screw

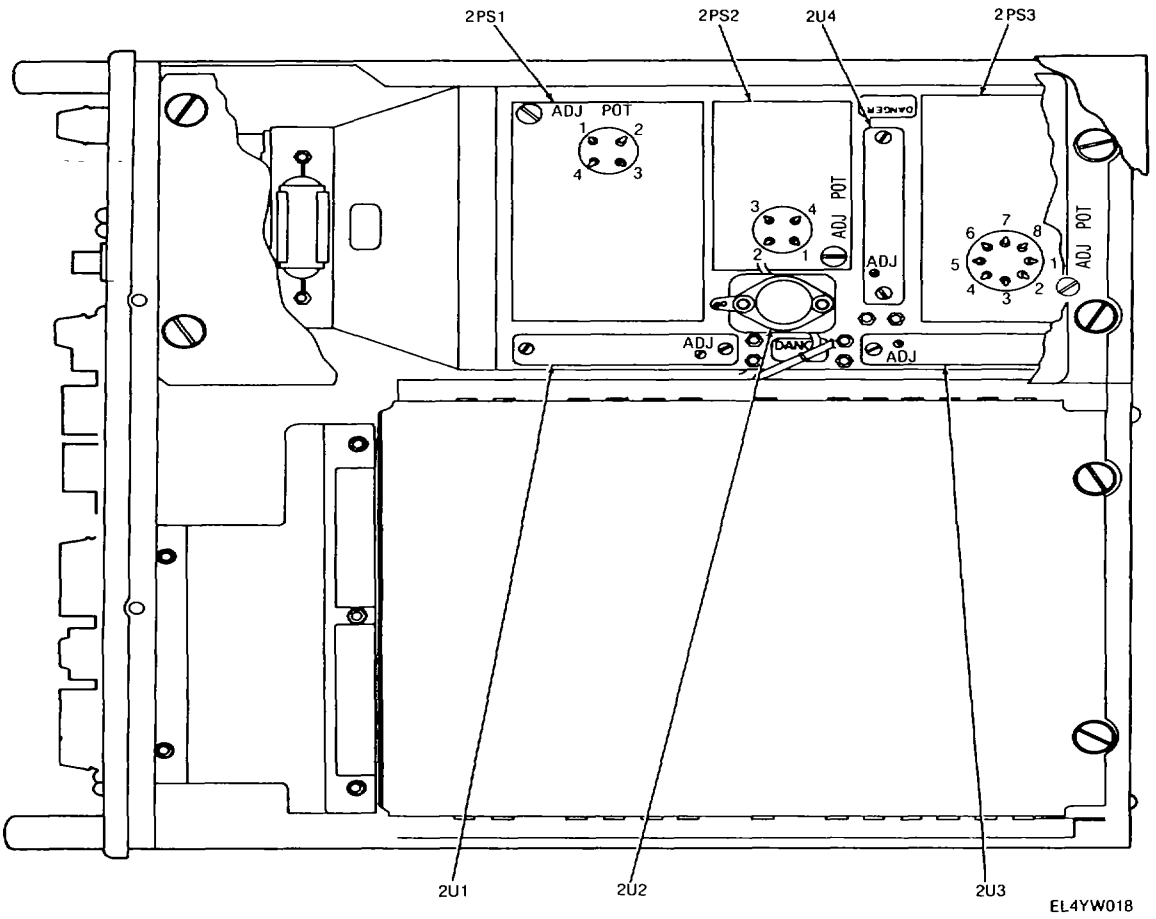


Figure 3-7. Power supply adjustments and test point locations.

(5) Connect the DVM between terminals 3 and 4 (gnd) on power supply 2PS3

(6) Set the data link control POWER switch to STBY

(7) Slowly adjust overvoltage protector 2U3 ADJ potentiometer counterclockwise (ccw) until the + 12 volt supply short-circuits

(8) Set the data link control POWER switch to OFF and adjust 2U3 ADJ potentiometer clockwise three and one half turns Overvoltage protector 2U3 is now set to trip at + 14 7 volts.

(9) Connect the DVM between terminals 5 and 4 (gnd) on power supply 2PS3

(10) Set the data link control POWER switch to STBY

(11) Slowly adjust overvoltage protector 2U4 ADJ potentiometer counterclockwise (ccw) until the -12 volt supply short-circuits.

(12) Set the data link control POWER switch to OFF and adjust 2U4 ADJ potentiometer clockwise three and one half turns Overvoltage protector 2U4 is now set to trip at - 14.7 volts

(13) Turn off all equipment power and disconnect test setup

3-22. Cleaning

WARNING

Adequate ventilation should be provided while using TRICHLOROTRIFLUORO-ETHANE. Prolonged breathing of vapor should be avoided The solvent should not be used near heat or open flame, the products of

decomposition are toxic and irritating. Since TRICHLOROTRIFLUOROETHANE dissolves natural oils, prolonged contact with skin should be avoided. When necessary, use gloves which the solvent cannot penetrate. If the solvent is taken internally, consult a physician immediately

Cleaning of the encoder and data link control is limited to removal of surface stains and dust accumulations. Remove surface stains using a lint-free cloth moistened with TRICHLOROTRIFLUOROETHANE cleaning compound. After cleaning with TRICOLOR TRIFLUOROETHANE, dry the area thoroughly with low pressure, filtered compressed air. Remove dust and other loose material from inside the equipment using a shop vacuum cleaner or soft bristle brush

3-23. Repainting and Refinishing

The extent of repainting and refinishing is limited to filling-in scratched or chipped surfaces on the encoder and data lhnk control Prior to painting, the damaged area should be thoroughly cleaned (para 3-22). Paint should be applied evenly with an artists brush Where bare metal is exposed, a primer coat should be applied first Light sanding may also be performed to smooth edges around the damaged area, as necessary The materials required for repainting and refinishing are listed m paragraph 3-5. Refer to TB 43-0118 for detailed instructions on repainting and refinishing electronic equipment

Section V. DIRECT SUPPORT TESTING PROCEDURES

3-24. General

This section contains procedures for physically testing the encoder and data link control. Functional tests for the encoder circuit cards are also presented. Refer to TM 11-5841-286-13 for inspection and testing of Radio Set AN/ARC-164(V)16.

3-25. Physical Inspection

WARNING

Disconnect power from the equipment before performing physical inspection procedures. Failure to comply could result in electrical shock injury to personnel.

Table 3-3 providers physical inspection procedures for the encoder and data link control. The physical inspection procedures are to be accomplished before the encoder circuit card tests (para 3-26).

Table 3-3. Physical inspection Procedure

Item to be Inspected	*Procedure*	*Standard*
All exterior surfaces	Check for stains, fungus and corrosion	Surfaces shall be free of stains, fungus and corrosion
Chassis	Check for dents, cracks and general structural damage	Chassis shall be free of structural damage
Painted surfaces.	Check for scratches and cracked or peeling pint.	All painted surfaces shall be free of scratches which penetrate the pant, and cracked or peeling pant
Screws, bolts and nuts	. Check for loose or missing screws, bolts and nuts.	All screws, bolts and nuts shall be tight, none shall be missing
Front panel switches.	Check for loose or missing knobs and normal switch action	Switch knobs shall be tight and mechanical action normal
Front panel indicators.	Check for burned-out or missing bulbs	Indicator bulbs shall be installed and m working order
Fuses and fuseholders	Check for burned-out or missing fuses	Fuses shall be installed and m working order
Electrical components	Check for signs of heat damage (charing discoloration)	Electrical components shall be free of heat damage
Connectors	Check for bent, broken or missing pms	All connector pins shall be straight and undamaged
Wiring	Check for breaks and damaged or frayed insulation	All wiring shall be free of damage to insulation and conductors

3-26. Testing Encoder Circuit Cards

a. General. Functional tests for the encoder circuit cards are presented in the following paragraphs. These go/no-go tests provide positive indication of circuit card performance. Table 3-4 lists the circuit cards to be tested and their referenced paragraphs Refer to paragraph 3-11 for encoder circuit card removal and replacement procedures If a fault (nogo indication) is indicated, remove the defective card from the test setup and return it to the depot for repair.

Table 3-4. Encoder Circut Cards to be Tested

Circuit cord	Reference designation	Reference paragraph
Analog-digital converter	2A2	3-27
FT accumulator memory	2A3/2A4	3-28
MT accumulator memory	2A512A6	3-29
Videocontrol	2A7	3-30
Videomultiplexer	2A9	3-31
MPU/tlmmg	2A11	3-32
Output buffer	2A12	3-33
Power fault detector	2A13	3-34
Output memory	2A14	3-35
ADAS control	2A16	3-36
Video interface	2A17	3-37

b. Test Equipment Required. Test equipment required for encoder circuit card testing is listed in table 3-5

Table 3-5. Test Equipment Required For Circuit Card Testing

Test Equipment	Common name
Test Set, Electronic Systems TS-3796/UKM-4	Control Interface unit
Systems Test Set, Electronic Systems, ANFUYM-7	Digital tester
Power Supply PP-3940/G	Power supply
Oscilloscope AN/USM-281C	Oscilloscope
Digital Voltmeter AN/GSM-64B	Digital voltmeter (DVM)
Extender Card, Video Encoder SM-D-94243-1	Extender card
Data recording-programmed magnetic cards as follows	
SM-A-942405	A2 program Card
SM-A-942355	A31A4 program card
SM-A-942360	A51A6 program card
SM-A-942410-1	A7programcardno 1
SM-A-942410-2	A7 program card no 2
SM-A-942365	A9 program card
SM-A-942385	All program card
SM-A-942445-1	A12 program card no 1
SM-A-942445-2	A12 program card no 2
SM-A-942445-3	A12 program card no 3
SM-A-942445-4	A12 program card no 4
SM-A-942445-5	A12 program card no 5
SM-A-942465-1	A13 program card no 1
SM-A-942465-2	A13 program card no 2
SM-A-942465-3	A13 program card no 3
SM-A-942370-1	A14 program card no 1
SM-A-942370-2	A14 program card no 2
SM-A-942450-1	A16 program card no 1
SM-A-942450-2	A16 program card no 2
SM-A-942450-3	A16 program card no 3
SM-A-942450-4	A16 program card no 4
SM-A-942450-5	A16 program card no 5
SM-A-942440-1	A17 program card no 1
SM-A-942440-2	A17 program card no 2
SM-A-942440-3	A17 program card no 3

3-27. Testing Analog-Digital Converter 2A2

a. Test Setup. Connect the equipment as shown m figure 3-8.

b. Preliminary Control Settings Prior to testing the circuit card, set the equipment controls as follows:

Control	*Setting*
Control Interface unit	
POWER ON/OFF	OFF
MODE SELECT	POWER OFF
Digital tester	
POWER	Down (off)
UUT POWER	Down (off)
TEST RATE PER SEC	1M
NUMBER OF TESTS	2M
DISPLAY	PROBE
PROBETHRESHOLD	2V

c. Test Procedure. Perform the following steps in the sequence given. Change equipment control settings only when instructed in the test procedure.

(1) Insert the encoder extender card into the MODULE TEST circuit card rack connector J1 on the control interface unit.

(2) Insert 2A2 card into the extender card.

(3) Connect +5 V power supply positive lead to pin 85 on extender card and negative lead to pin 86. Using the digital voltmeter, adjust power supply for 0.28 + 0.01 V dc.

(4) Insert A2 program card (SM-A-942405) into the card reader slot on the digital tester.

(5) On the control interface unit, set the POWER ON/OFF switch to ON and the MODE SELECT switch to MODULE TEST ENC. Verify that the MODE/ POWER MODULE TEST ON green indicator lamp is illuminated

NOTE

The MODE/POWER SHORT red indicator lamp will be illuminated at this time, but will be extinguished when the digital tester UUT POWER switch is set to the ON position in the following step.

(6) On the digital tester, set the POWER and UUT POWER switches to the on positions (up). Verify that the red indicator lamps for these switches are illuminated and the MODE/POWER SHORT lamp is off.

(7) On the digital tester, load the program on the A2 program card into the digital tester memory by pressing the PROGRAM ENTER momentary switch to the down position

NOTE

The PROGRAM ENTER red indicator lamp will be illuminated during the program enter period.

(8) Verify that the READY/ERROR white indicator lamp on the digital tester illuminates when the program has been entered (9) Depress the CONT TEST switch on the digital tester (10) Connect the positive lead of the digital volt-meter to test point Jl-1 and the negative lead to J1-22 (fig 3-9)

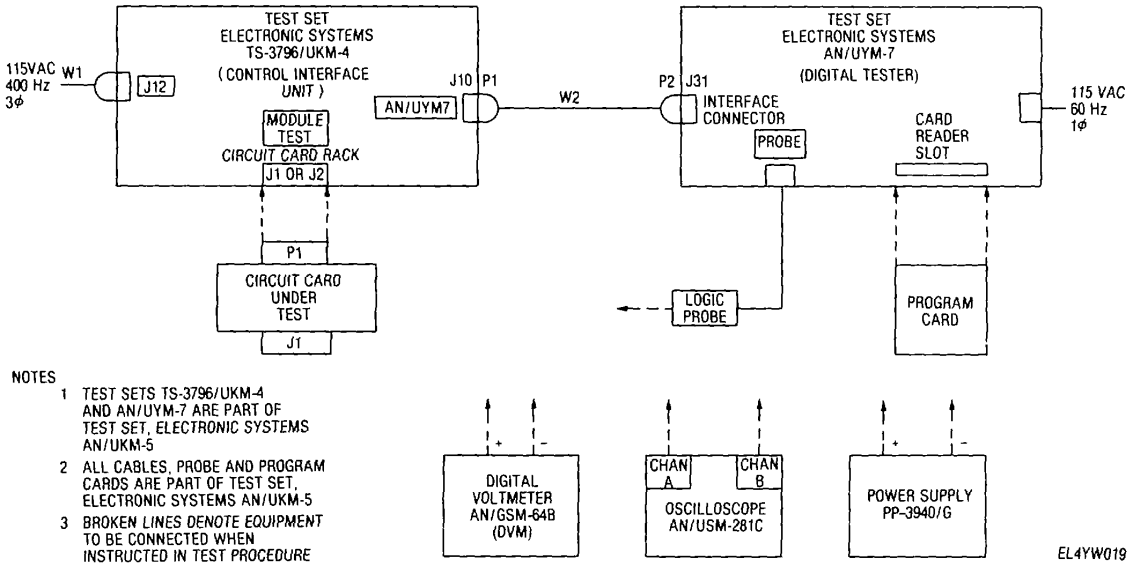


Figure 3-8. Typical test setup for circuit card testing

(11) Verify an indication of 4 O 0 01 V dc

(12) Connect the positive lead of the digital volt meter to pin 85 and negative lead to pin 86 on the ex-tender card (This Is the monitor point for the output voltage of the power supply.)

(13) Adjust power supply output to voltage listed tester logic probe to each pin listed m table headings in the first column of table 3-6 Then, connect digital on right side of table.

NOTE

A logic "1" in the table will be Indicated by the probe light illuminating. A logic "0" is indicated by the probe light being off. Dut to internal noise from the digital tester, some levels may be intermittent Look for the most

(14) Verify that all six logic levels are correct for common value such power supply setting in table 3-6

Table 3-6. MT Channel lA/D Levels

Power supply settings(V)	*Output logic levels*					
	J1-V	*J1-20*	*J1-S*	*J1-17*	*J1-U*	*J1-18*
0.28	0	0	0	0	0	0
0.88	0	0	1	0	0	1
1.43	0	1	0	0	1	0
2.00	0	1	1	0	1	1
2.57	1	0	0	1	0	0
3.14	1	0	1	1	0	1
3.71	1	1	0	1	1	0
4.30	1	1	1	1	1	1

(15) Adjust power supply to 0 06 V dc Disconnect power supply and digital voltmeter

(16) Connect the positive leads of the power supply and digital voltmeter to pm 3 on the extender card

(17) Connect the negative leads of the power supply and digital voltmeter to pin 4 on the extender card

(18) Repeat steps 13 and 14 while verifying that all ten logic levels are correct as per table 3-7

Table 3-7. FT Channel A/D Levels

Power supply	*Output logic levels*									
settings (V)	*J1-P*	J1-W	*J1-N*	*J1-T*	*J1-R*	*J1-19*	*J1-K*	*J1-W*	*J1-16*	*J1-L*
0.06	0	0	0	0	0	0	0	0	*0*	0
0.19	0	0	0	0	1	0	0	0	0	1
0.32	0	0	0	1	0	0	0	0	1	0
0.45	0	0	0	1	1	0	0	0	1	1
0.58	0	0	1	0	0	0	0	1	0	0
0.70	0	0	1	0	1	0	0	1	0	1
0.84	0	0	1	1	0	0	0	1	1	0
0.95	0	0	1	1	1	0	0	1	1	1
1.09	0	1	0	0	0	0	1	0	0	0
1.22	0	1	0	0	1	0	1	0	0	1
1.39	0	1	0	1	0	0	1	0	1	0
1.47	0	1	0	1	1	0	1	0	1	1
1.61	0	1	1	0	0	0	1	1	0	0
1.73	0	1	1	0	1	0	1	1	0	1
1.86	0	1	1	1	0	0	1	1	1	0
1.98	0	1	1	1	1	0	1	1	1	1
2.12	1	0	0	0	0	1	0	0	0	0
2.25	1	0	0	0	1	1	0	0	0	1
2.38	1	0	0	1	0	1	0	0	1	0
2.51	1	0	0	1	1	1	0	0	1	1
2.63	1	0	1	0	0	1	0	1	0	0
2.77	1	0	1	0	1	1	0	1	0	1
2.89	1	0	1	1	0	1	0	1	1	0
3.01	1	0	1	1	1	1	0	1	1	1
3.18	1	1	0	0	0	1	1	0	0	0
3.28	1	1	0	0	1	1	1	0	0	1
3.42	1	1	0	1	0	1	1	0	1	0
3.54	1	1	0	1	1	1	1	0	1	1
3.68	1	1	1	0	0	1	1	1	0	0
3.80	1	1	1	0	1	1	1	1	0	1
3.93	1	1	1	1	0	1	1	1	1	0
4.06	1	1	1	1	1	1	1	1	1	1

(19) Remove the probe tip from the circuit card test point and set the POWER switches on the equipment to their off positions Remove the circuit card under test, extender card, and the program card from the test setup

3-28. Testing FT Accumulator Memory 2A3/2A4

a. Test Setup Set all equipment POWER switches to OFF. Connect the equipment as shown in figure 3-8.

b. Preliminary Control Settings Prior to testing the circuit card, set the equipment controls as follows.

Control	*Setting*
Control Interface unit	
POWER ON/OFF	OFF
MODE SELECT	POWER OFF
Digital tester	
POWER	Down (off)
UUT POWER	Down (off)
TEST RATE PER SEC	400K
NUMBER OF TESTS	2M
DISPLAY	PASS/FAIL
PROBE THRESHOLD	2V

c. Test Procedure. Perform the following steps in the sequence given Change equipment control settings only when instructed In the test procedure

(1) Insert the circuit card to be tested into the MODULE TEST circuit card rack connector J1 on the control interface unit

(2) Insert A3/A4 program card (SM-A-942355) into the card reader lot on the digital tester

(3) On the control Interface unit, set the POWER ON/OFF switch to ON and the MODE SELECT switch to MODULE TEST ENC Verify that the MODE/POWER MODULE TEST ON green Indicator lamp is illuminated.

NOTE

The MODE/POWER SHORT red indicator lamp will be illuminated at this time, but will be extinguished when the digital tester UUT POWER switch is set to the ON position in the following step

(4) On the digital tester, set the POWER and UUT POWER switches to the on positions (up). Verify that the red indicator lamps for these switches are illuminated and the MODE/POWER SHORT lamp is off

(5) On the digital tester, load the program on the A3/A4 program card into the digital tester memory by

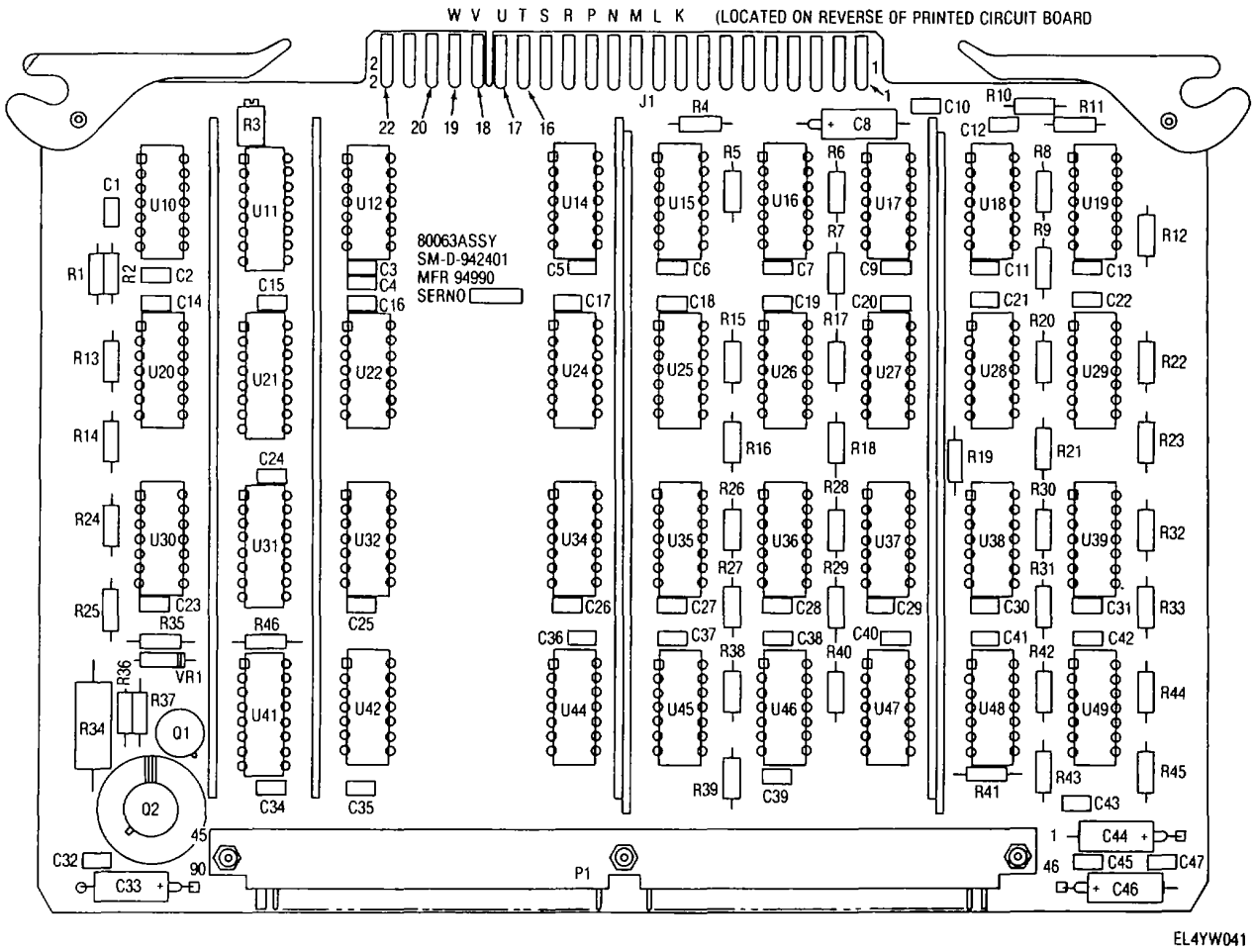


Figure 3-9. Analog-digital converter 2A2 test point locations.

pressing the PROGRAM ENTER momentary switch to the down position

NOTE

The PROGRAM ENTER red indicator lamp will be illuminated during the program enter period

(6) Verify that the READY/ERROR white indicator lamp on the digital tester illuminates when the program has been entered

(7) Initiate a complete test sequence by pressing either one of the TEST momentary switches to the down position

NOTE

The TEST red indicator lamp for the switch selected will be illuminated while the test is in progress

(8) Initiate a second test by repeating step (7) above Verify that the green PASS Indicator lamp on the digital tester illuminates at the completion of the second test

(9) Set the POWER switches on the equipment to their off positions Remove the circuit card under test and the program card from the test setup.

3-29. Testing MT Accumulator Memory 2A5/2A6

a. Test Setup Connect the equipment as shown in figure 3-10

b. Preliminary Control Settings. Prior to testing the circuit card, set the equipment controls as follows.

Control	*Setting*
Control Interface unit	
POWER ON/OFF	OFF
MODE SELECT	POWER OFF
Digital tester	
POWER	Down (off)
UUT POWER	Down (off)
TEST RATE PER SEC	400K
NUMBER OF TESTS	2M
DISPLAY	PASS/FAIL
PROBE THRESHOLD	2V

c. Test Procedure Perform the following steps in the sequence given Change equipment control settings only when instructed in the test procedure

(1) Insert the circuit card to be tested into the MODULE TEST circuit card rack connector J1 on the control interface unit Connect cable W3 to circuit card connector J1.

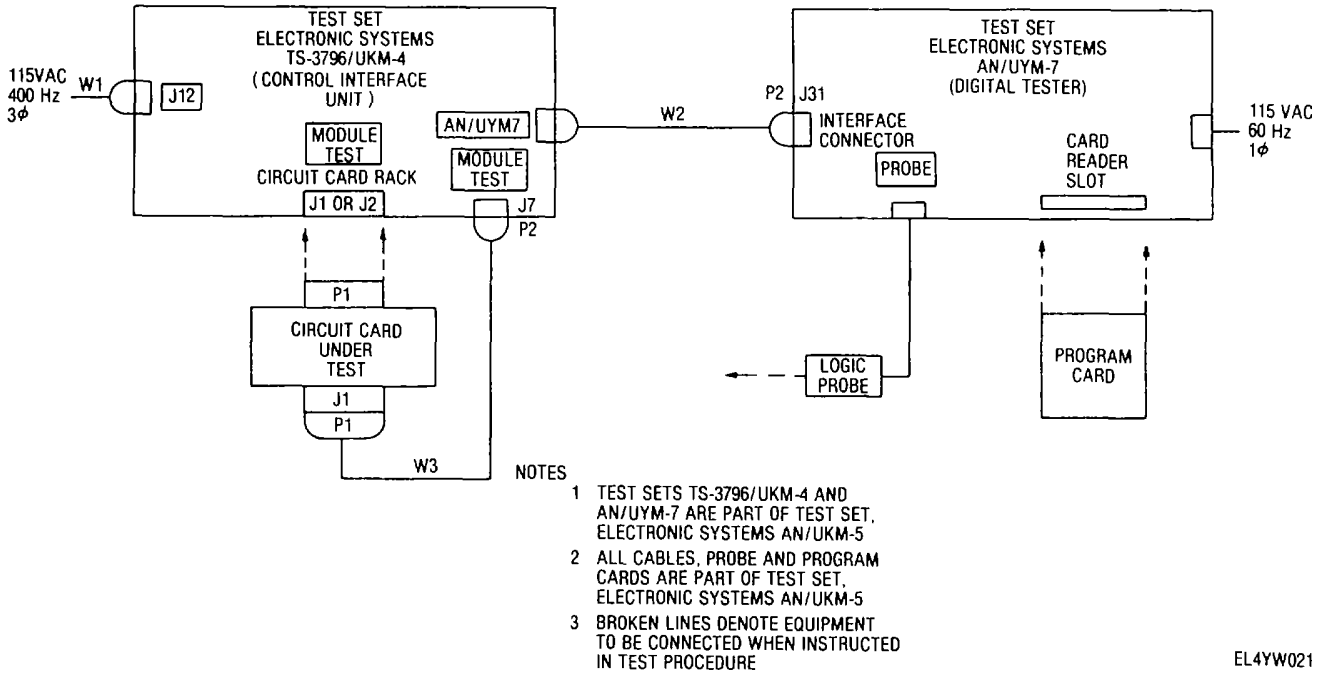


Figure 3-10. Test setup for circuit card testing utilizing cable W3.

(2) Insert A5/A6 program card (SM-A-942360) into the card reader slot on the digital tester

(3) On the control Interface unit, set the POWER ON/OFF switch to ON and the MODE SELECT switch to MODULE TEST ENC. Verify that the MODE/POWER MODULE TEST ON green indicator lamp is illuminated.

NOTE

The MODE/POWER SHORT red indicator lamp will be illuminated at this time, but will be extinguished when the digital tester UUT POWER switch is set to the on position in the following step

(4) On the digital tester, set the POWER and UUT POWER switches to the on positions (up) Verify that the red indicator lamps for these switches are illuminated and the MODE/POWER SHORT lamp is off

(5) On the digital tester, load the program on the A5/A6 program card into the digital tester memory by pressing the PROGRAM ENTER momentary switch to the down position

NOTE

The PROGRAM ENTER red indicator lamp will be illuminated during the program enter period

(6) Verify that the READY/ERROR white indicator lamp on the digital tester illuminates when the program has been entered

(7) Initiate a complete test sequence by pressing either one of the TEST momentary switches to the down position

NOTE

The TEST red indicator lamp for the switch selected will be illuminated while the test is in progress

(8) Imitate a second test by repeating step (7) above. Verify that the green PASS indicator lamp on the digital tester illuminates at the completion of the second test

(9) Set the TEST RATE PER SEC switch on the digital tester to 1M

(10) Refer to figure 3-11 for test point locations and connect channel A of the oscilloscope between test points U44-15 and J1-22 (gnd)

(11) Adjust oscilloscope for positive trigger, 2V/division vertical, and 10 microseconds/division horizontal

(12) Depress the CONT TEST switch on the digital tester Verify that the display on channel A of the oscilloscope consists of both logic "1"s and "0's

(13) Set the POWER switches on the equipment to their off positions. Remove the circuit card under test and the program card from the test setup

3-30. Testing Video Control 2A7

a. Test Setup Connect the equipment as shown in figure 3-8 *b Preliminary Control Settings.* Prior to testing the circuit card, set the equipment controls as follows:

Control	*Setting*
Control Interface unit	
POWER ON/OFF	OFF

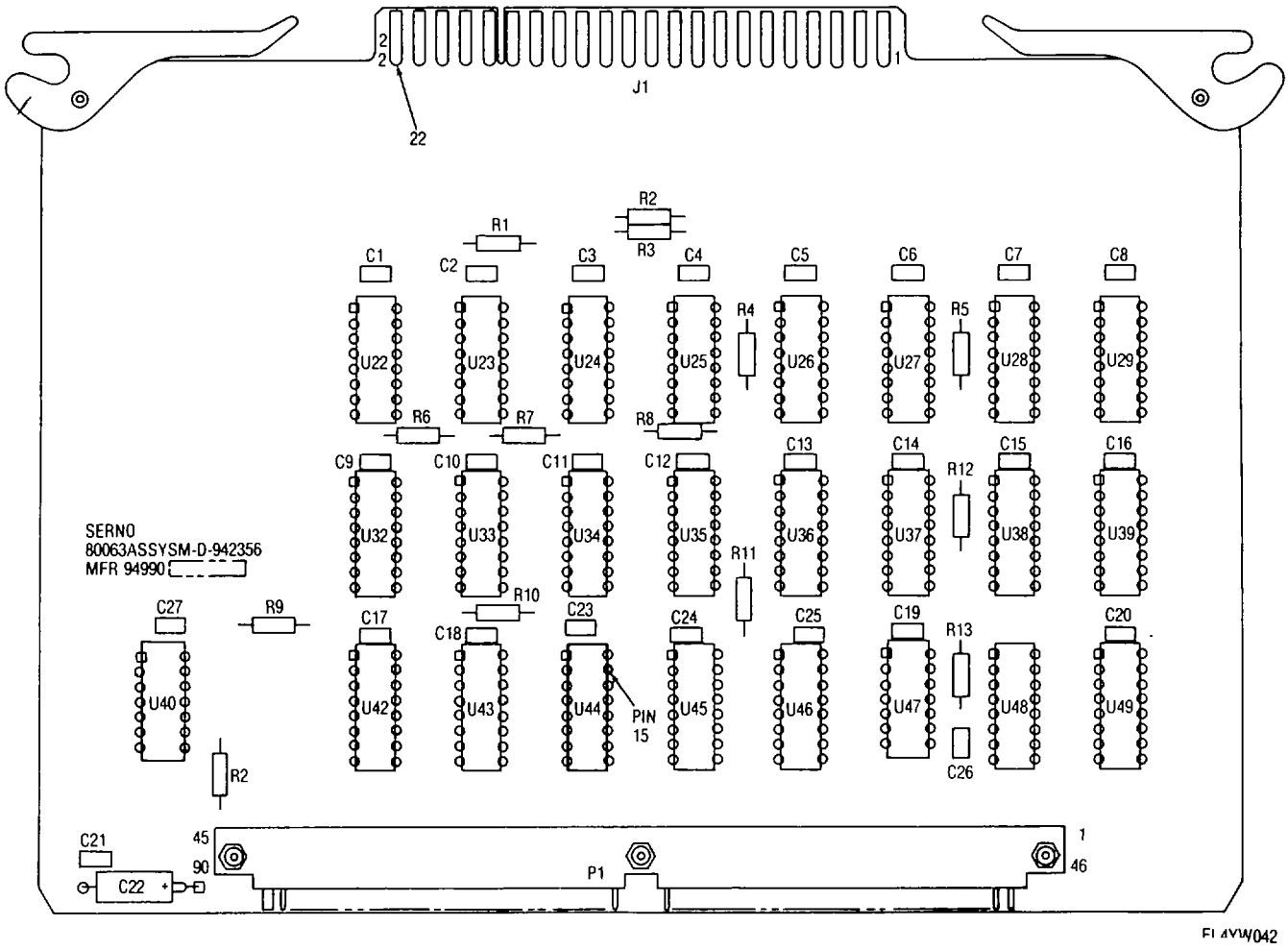


Figure 3-11. MT accumulator memory 2A5/2A6 test point locations.

Control	*Setting*
MODE SELECT	POWER OFF
Digital tester	
POWER	Down (off)
UUT POWER	Down (off)
TEST RATE PER SEC	2M
NUMBER OF TESTS	10M
DISPLAY	PASS/FAIL
PROBE THRESHOLD	2V

c. Test Procedure Perform the following steps in the sequence given. Change equipment control settings only when instructed m the test procedure

(1) Insert the circuit card to be tested into the MODULE TEST circuit card rack connector J1 on the control interface unit

(2) Insert A7 program card no 1 (SM-A-942410-1) into the card reader slot on the digital tester

(3) On the control interface unit, set the POWER ON/OFF switch to ON and the MODE SELECT switch to MODULE TEST ENC Verify that the MODE/POWER MODULE TEST ON green indicator lamp is illuminated.

NOTE

The MODE/POWER SHORT red indicator lamp will be illuminated at this time, but will be extinguished when the digital tester UUT POWER switch is set to the ON position in the following step

(4) On the digital tester, set the POWER and UUT POWER switches to the on positions (up) Verify that the red indicator lamps for these switches are illuminated and the MODE/POWER SHORT lamp is off

(5) On the digital tester, load the program on the A7 program card no 1 mto the digital tester memory by pressing the PROGRAM ENTER momentary switch to the down position

NOTE

The PROGRAM ENTER red indicator lamp will be illuminated during the program enter period

(6) Verify that the READY/ERROR white indicator lamp on the digital tester illuminates when the pro-gram has been entered

(7) Initiate a complete test sequence by pressing

either one of the TEST momentary switches to the down position

NOTE

The TEST red indicator lamp for the switch selected will be illuminated while the test is in progress

(8) Initiate a second test by repeating step (7) above Verify that the green PASS indicator lamp on the digital tester Illuminates at the completion of the second test

(9) Remove A7 program card no 1 from the card reader slot on the digital tester

(10) Insert A7 program card no 2 (SM-A-942410-2) into the card reader slot

(11) Set the TEST RATE PER SEC switch on the digital tester to 1M

(12) On the digital tester, load the program on the A7 program card no 2 into the digital tester memory by pressing the PROGRAM ENTER momentary switch to the down position

(13) Verify that the READY/ERROR white indicator lamp on the digital tester illuminates when the program has been entered

(14) Initiate a complete test sequence by pressing either one of the TEST momentary switches to the down position

(15) Initiate a second test by repeating step (14) above Verify that the green PASS indicator lamp on the digital tester illuminates at the completion of the second test

(16) Set the DISPLAY switch on the digital tester to PROBE

(17) Refer to figure 3-12 for test point locations and connect the logic probe to U10 pin 4, on the circuit card under test

(18) Initiate a test by pressing down on the digital tester TEST switch Verify that the probe tip lamp flashes during the test

(19) Remove the logic probe tip from U10 pin 4 and connect it to U10, pin 12

(20) Repeat step (18) above

(21) Remove the probe tip from the circuit card test point and set the POWER switches on the equip-ment to their off positions Remove the circuit card under test and the program card from the test setup

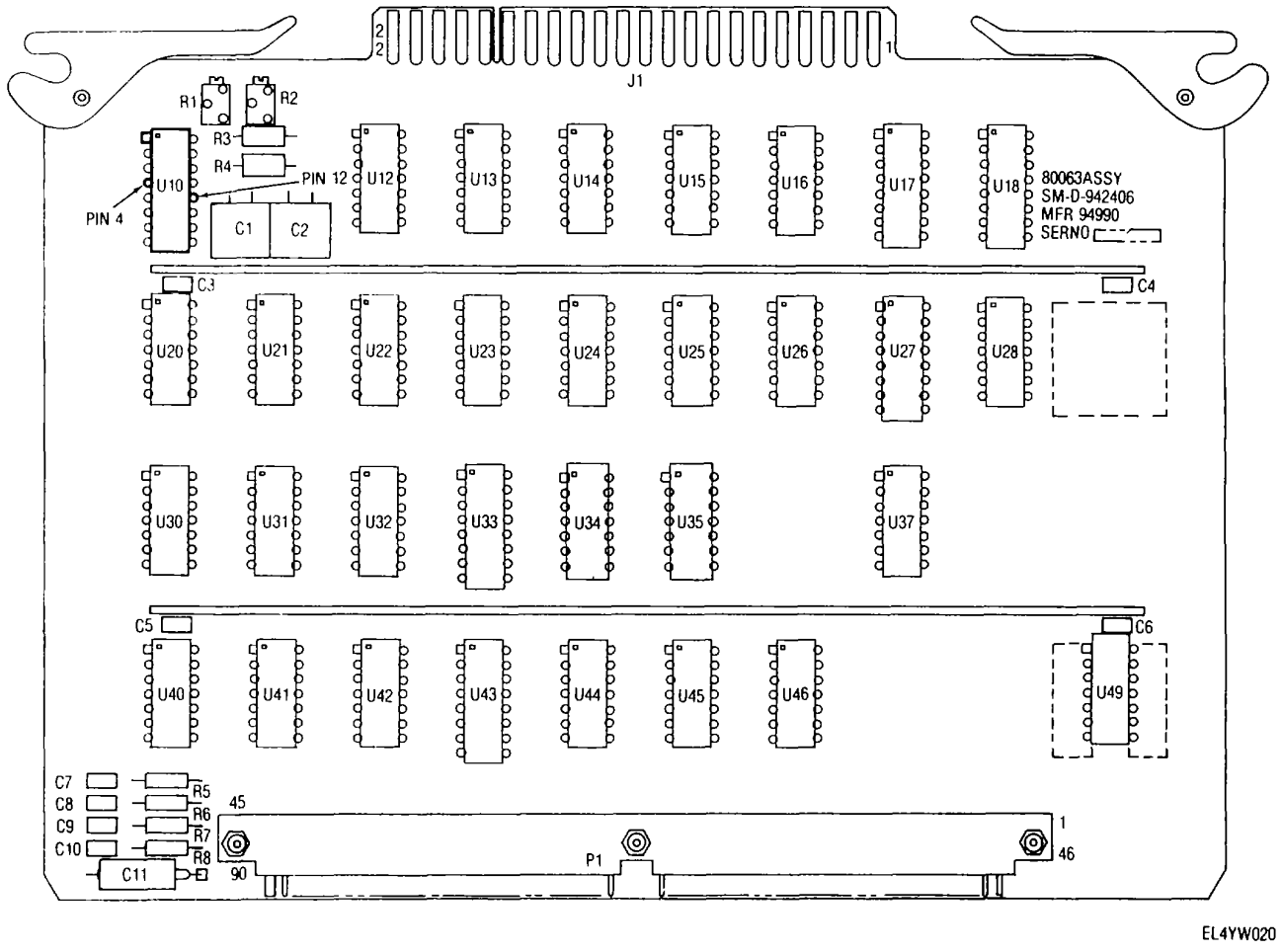


Figure 3-12. Video control 2A7 test point locations.

3-31. Testing Video Multiplexer 2A9

a. Test Setup. Connect the equipment as shown in figure 3-10

b. Preliminary Control Settings. Prior to testing the circuit card, set the equipment controls as follows.

Control	*Setting*
Control interface unit	
POWER ON/OFF	OFF
MODE SELECT	POWER OFF
Digital tester	
POWER	Down (off)
WT POWER	Down (off)
TEST RATE PER SEC	100K
NUMBER OF TESTS	1M
DISPLAY	PASS/FAIL
PROBE THRESHOLD	2V

c. Test Procedure. Perform the following steps In the sequence given. Change equipment controls only when instructed in the test procedure

(1) Verify that cable W3 is connected as shown in figure 3-10 and insert the circuit card to be tested into the MODULE TEST circuit card rack connector J1 on the control interface unit

(2) Insert A9 program card (SM-A-942365) into the card reader slot on the digital tester

(3) On the control interface unit, set the POWER ON/OFF switch to ON and the MODE SELECT switch to MODULE TEST ENC Verify that the MODE/POWER MODULE TEST ON green indicator lamp is illuminated

NOTE

The MODE/POWER SHORT red indicator lamp will be illuminated at this time, but will be extinguished when the digital tester UUT POWER switch is set to the on position in the following step

(4) On the digital tester, set the POWER and UUT POWER switches to the on positions (up) Verify that the red indicator lamps for these switches are illuminated and the MODE/POWER SHORT lamp is off

(5) On the digital tester, load the program on the A9 program card into the digital tester memory by pressing the PROGRAM ENTER momentary switch to the down position.

NOTE

The PROGRAM ENTER red indicator lamp will be illuminated during the program enter period

(6) Verify that the READY/ERROR white indicator lamp on the digital tester illuminates when the program has been entered

(7) Initiate a complete test sequence by pressing either one of the TEST momentary switches to the down position

NOTE

The TEST red indicator lamp for the switch selected will be illuminated while the test is in progress.

(8) Initiate a second test by repeating step (7) above Verify that the green PASS indicator lamp on the digital tester illuminates at the completion of the second test

(9) Set the POWER switches on the equipment to their off positions Remove the circuit card under test and the program card from the test setup

3-32. Testing MPU/Timing 2A11

a. Test Setup Connect the equipment as shown in figure 3-8

b. Preliminary Control Settings Prior to testing the circuit card, set the equipment controls as follows

Control	Setting
Control interface unit	
POWER ON/OFF	OFF
MODE SELECT	POWER OFF
Digital tester	
POWER	Down (off)
UUT POWER	Down (off)
TEST RATE PER SEC	2M
NUMBER OF TESTS	20M
DISPLAY	PASS/FAIL
PROBETHRESHOLD	2V

c. Test Procedure Perform the following steps in the sequence given Change equipment control settings only when instructed in the test procedure

(1) Insert the circuit card to be tested into the MODULE TEST circuit card rack connector J2 on the control interface unit

(2) Insert All program card (SM-A-942385) into the card reader slot on the digital tester.

(3) On the control interface unit, set the POWER ON/OFF switch to ON and the MODE SELECT switch to MODULE TEST ENC. Verify that the MODE/POWER MODULE TEST ON green indicator lamp is illuminated

NOTE

The MODE/POWER SHORT red indicator lamp will be illuminated at this time, but will be extinguished when the digital tester UUT POWER switch is set to the on position in the following step

(4) On the digital tester, set the POWER and UUT POWER switches to the on positions (up) Verify that the red indicator lamps for these switches are illuminated and the MODE/POWER SHORT lamp is off.

(5) On the digital tester, load the program on the All program card into the digital tester memory by pressing the PROGRAM ENTER momentary switch to the down position

NOTE

The PROGRAM ENTER red indicator lamp will be illuminated during the program enter period.

(6) Verify that the READY/ERROR white indicator lamp on the digital tester illuminates when the program has been entered

(7) Initiate a complete test sequence by pressing either one of the TEST momentary switches to the down position

NOTE

The TEST red indicator lamp for the switch selected will be illuminated while the test is in progress

(8) Initiate a second test by repeating step (7) above Verify that the green PASS indicator lamp on the digital tester illuminates at the completion of the second test.

(9) Set the DISPLAY switch on the digital tester to PROBE.

(10) Refer to figure 3-13 for test point locations and connect the logic probe to each test point listed below While monitoring each test point, initiate a test by pressing down on the digital tester TEST switch Verify that the correct corresponding transition counts are displayed on the digital tester counter, or that the probe flashes as follows'

Test Point	*Count*
U48-11	Flashing
U48-12	Flashing
U49-12	Flashing
U49-13	563
U47-13	Flashing
U28-12	1875370

(11) Remove the probe tip from the circuit card test point and set the POWER switches on the equipment to their off positions. Remove the circuit card under test and the program card from the test setup

3-33. Testing Output Buffer 2A12

a. Test Setup Connect the equipment as shown in figure 3-8.

b. Preliminary Control Settings Prior to testing the circuit card, set the equipment controls as follows

Control	*Setting*
Control interface unit	
POWER ON/OFF	OFF
MODE SELECT	POWER OFF
Digital tester	
POWER	Down (off)
UUT POWER	Down (off)
TEST RATE PER SEC	200K
NUMBER OF TESTS	2M
DISPLAY	PASS/FAIL
PROBETHRESHOLD	2V

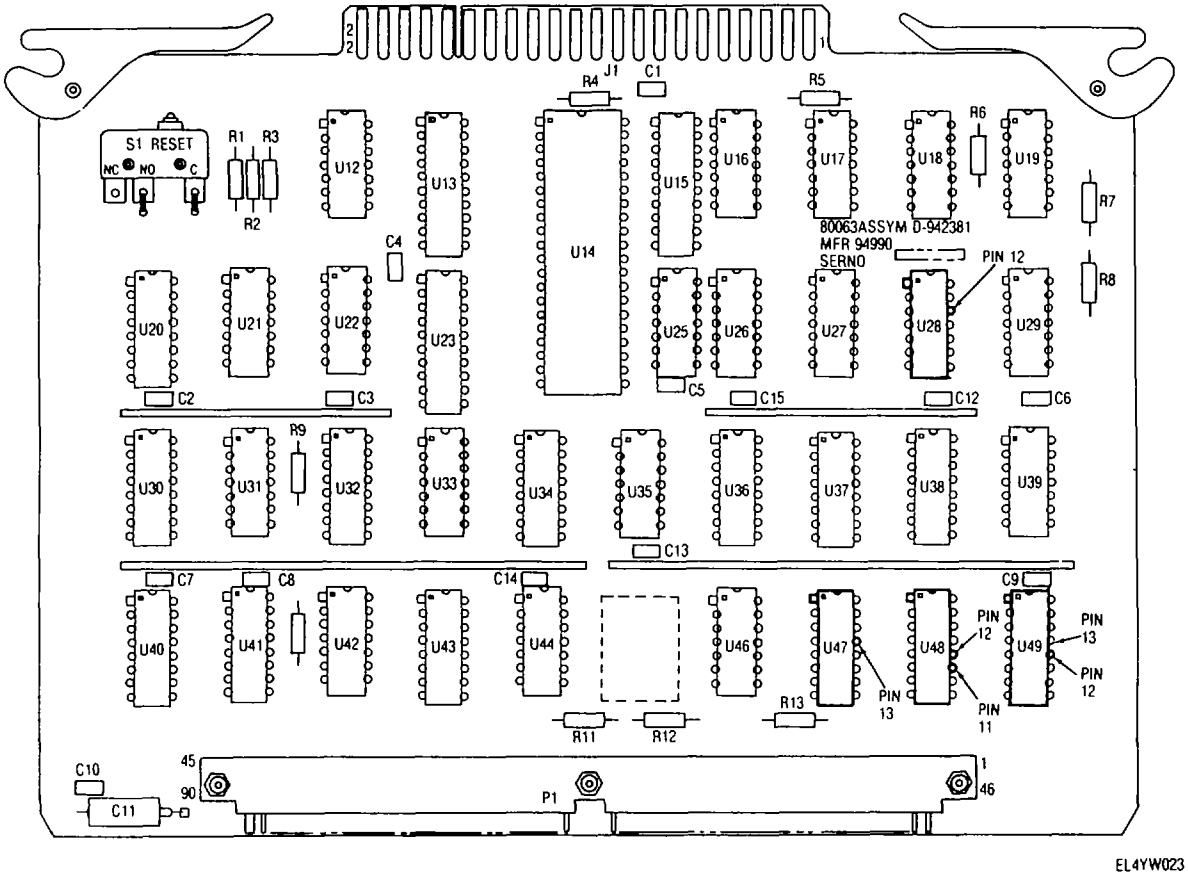


Figure 3-13. MPU/timing 2A11 test point locations.

c. Test Procedure Perform the following steps in the sequence given Change equipment control settings only when instructed in the test procedure.

(1) Insert the circuit card to be tested into the MODULE TEST circuit rack connector J1 on the control interface unit

(2) Insert A12 program card no.1 (SM-A-942445-1) into the card reader slot on the digital tester.

(3) On the control interface unit, set the POWER ON/OFF switch to ON and the MODE SELECT switch to MODULE TEST ENC. Verify that the MODE/POWER MODULE TEST ON green indicator lamp is illuminated

NOTE

The MODE/POWER SHORT red indicator lamp will be illuminated at this time, but will be extinguished when the digital tester UUT POWER switch is set to the ON position in the following step

(4) On the digital tester, set the POWER and UTT POWER switches to the on positions (up) Verify that the red indicator lamps for these switches are illuminated and the MODE/POWER SHORT lamp is off.

(5) On the digital tester, load the program on the A12 program card no 1 into the digital tester memory by pressing the PROGRAM ENTER momentary switch to the down position

NOTE

The PROGRAM ENTER red indicator lamp will be illuminated during the program enter period

(6) Verify that the READY/ERROR white indicator lamp on the digital tester illuminates when the program has been entered

(7) Initiate a complete test sequence by pressing either one of the TEST momentary switches to the down position.

NOTE

The TEST red indicator lamp for the switch selected will be illuminated while the test is in progress.

(8) Initiate a second test by repeating step (7) above Verify that the green PASS indicator lamp on the digital tester illuminates at the completion of the second test.

(9) Remove A12 program card no 1 from the card reader slot on the digital tester.

(10) Insert A12 program card no 2 (SM-A-942445-2) into the card reader slot

(11) On the digital tester, load the program on the A12 program card no. 2 into the digital tester memory by pressing the PROGRAM ENTER momentary switch to the down position

(12) Verify that the READY/ERROR white indicator lamp on the digital tester illuminates when the program has been entered

(13) Initiate a complete test sequence by pressing either one of the TEST momentary switches to the down position.

(14) Initiate a second test by repeating step (13) above. Verify that the green PASS indicator lamp on the digital tester illuminates at the completion of this second test

(15) Remove A12 program card no. 2 from the card reader slot on the digital tester.

(16) Insert A12 program card no 3 (SM-A-942445-3) into the card reader slot.

(17) Set the TEST RATE PER SEC switch on the digital tester to 1M

(18) On the digital tester, load the program on the A12 program card no 3 into the digital tester memory by pressing the PROGRAM ENTER switch to the down position.

(19) Verify that the READY/ERROR white indicator lamp on the digital tester illuminates when the program has been entered.

(20) Initiate a complete test sequence by pressing either one of the TEST switches to the down position.

(21) Initiate a second test by repeating step (20) above Verify that the green PASS indicator lamp on the digital tester illuminates at the completion of this test

(22) Remove A12 program card no. 3 from the card reader slot on the digital tester

(23) Insert A12 program card no 4 (SM-A-942445-4) into the card reader slot

(24) On the digital tester, load the program on the A12 program card no. 4 into the digital tester memory by pressing the PROGRAM ENTER switch to the down position

(25) Verify that the READY/ERROR white indicator lamp on the digital tester illuminates when the program has been entered.

(26) Initiate a complete test sequence by pressing either one of the TEST switches to the down position

(27) Initiate a second test by repeating step (26) above Verify that the green PASS indicator lamp illuminates at the completion of this test

(28) Remove A12 program card no. 4 from the card reader slot on the digital tester

(29) Insert A12 program card no. 5 (SM-A-942445-5) into the card reader slot.

(30) On the digital tester, load the program on the A12 program card no 5 into the digital tester memory by pressing the PROGRAM ENTER switch to the down position

(31) Verify that the READY/ERROR white indicator lamp on the digital tester illuminates when the program has been entered

(32) Initiate a complete test sequence by pressing either one of the TEST switches to the down position

(33) Initiate a second test by repeating step (32) above. Verify that the green PASS indicator lamp illuminates at the completion of this test.

(34) Set the POWER switches on the equipment to their off positions Remove the circuit card under test and the program card from the test setup.

3-34. Testing Power Fault Detector 2A13

a. Test Setup. Connect the equipment as shown in figure 3-10.

b. Preliminary Control Settings Prior to testing the circuit card, set the equipment controls as follows.

Control	Setting
Control interface unit	
POWER ON/OFF	OFF
MODE SELECT	POWER OFF
Digital tester	
POWER	Down (off)
UUT POWER	Down (off)
TEST RATE PER SEC	200K
NUMBER OF TESTS	1M
DISPLAY	PASS/FAIL
PROBE THRESHOLD	2V

c. Test Procedure. Perform the following steps in the sequence given. Change equipment control settings only when instructed in the test procedure

NOTE

The following test procedure tests only the digital functions of power fault detector 2A13

(1) Insert the circuit card to be tested into the MODULE TEST circuit card rack connector J1 on the control interface unit Connect cable W3 to circuit card connector J1.

(2) Insert A13 program card no 1 (SM-A-942465-1) into the card reader slot on the digital tester

(3) On the control interface unit, set the POWER ON/OFF switch to ON and the MODE SELECT switch to MODULE TEST ENC Verify that the MODE/POWER MODULE TEST ON green indicator lamp Is illuminated

NOTE

The MODE/POWER SHORT red indicator lamp will be illuminated at this time, but will be extinguished when the digital tester UUT POWER switch is set on the ON position in the following step.

(4) On the digital tester, set the POWER and UUT POWER switches to the on positions (up). Verify that the red indicator lamps for these switches are illuminated and the MODE/POWER SHORT lamp is off.

(5) On the digital tester, load the program on the A13 program card no. 1 into the digital tester memory by pressing the PROGRAM ENTER momentary switch to the down position.

NOTE

The PROGRAM ENTER red indicator lamp will be illuminated during the program enter period.

(6) Verify that the READY/ERROR white indicator lamp on the digital tester illuminates when the pro-gram has been entered.

(7) Initiate a complete test sequence by pressing either one of the TEST momentary switches to the down position.

NOTE

The TEST red indicator lamp for the switch selected will be illuminated while the test **is** in progress.

(8) Initiate a second test by repeating step (7) above Verify that the green PASS indicator lamp on the digital tester illuminates at the completion of the second test.

(9) Set the TEST RATE PER SEC switch on the digital tester to 2M

(10) Disconnect cable W3 from connector J1 of A13.

(11) Remove A13 program card no. 1 from the card reader slot on the digital tester

(12) Insert A13 program card no 2 (SM-A-942465-2) Into the card reader slot

(13) On the digital tester, load the program on the A13 program card no 2 into the digital tester memory by pressing the PROGRAM ENTER momentary switch to the down position

(14) Verify that the READY/ERROR white indicator lamp on the digital tester illuminates when the program has been entered

(15) Refer to figure 3-14 for test promt locations and connect channel A of the oscilloscope between test promts J1-14 and J1-22 (gnd).

(16) Connect channel B of the oscilloscope between test points P1-26 and J1-22 (gnd).

(17) Depress the CONT TEST switch on the digital tester Verify that the display on channels A and B of the oscilloscope are similar to that shown m view A of figure 3-15

(18) Remove A13 program card no. 2 from the card reader slot on the digital tester.

(19) Insert A13 program card no. 3 (SM-A-942465-3) into the card reader slot.

(20) On the digital tester, load the program on the A13 program card no 3 into the digital tester memory by pressing the PROGRAM ENTER momentary switch to the down position

(21) Verify that the READY/ERROR white indicator lamp on the digital tester illuminates when the program has been entered

(22) Depress the CONT TEST switch on the digital tester and verify that the display on channel A is similar to that shown m view B of figure 3-15

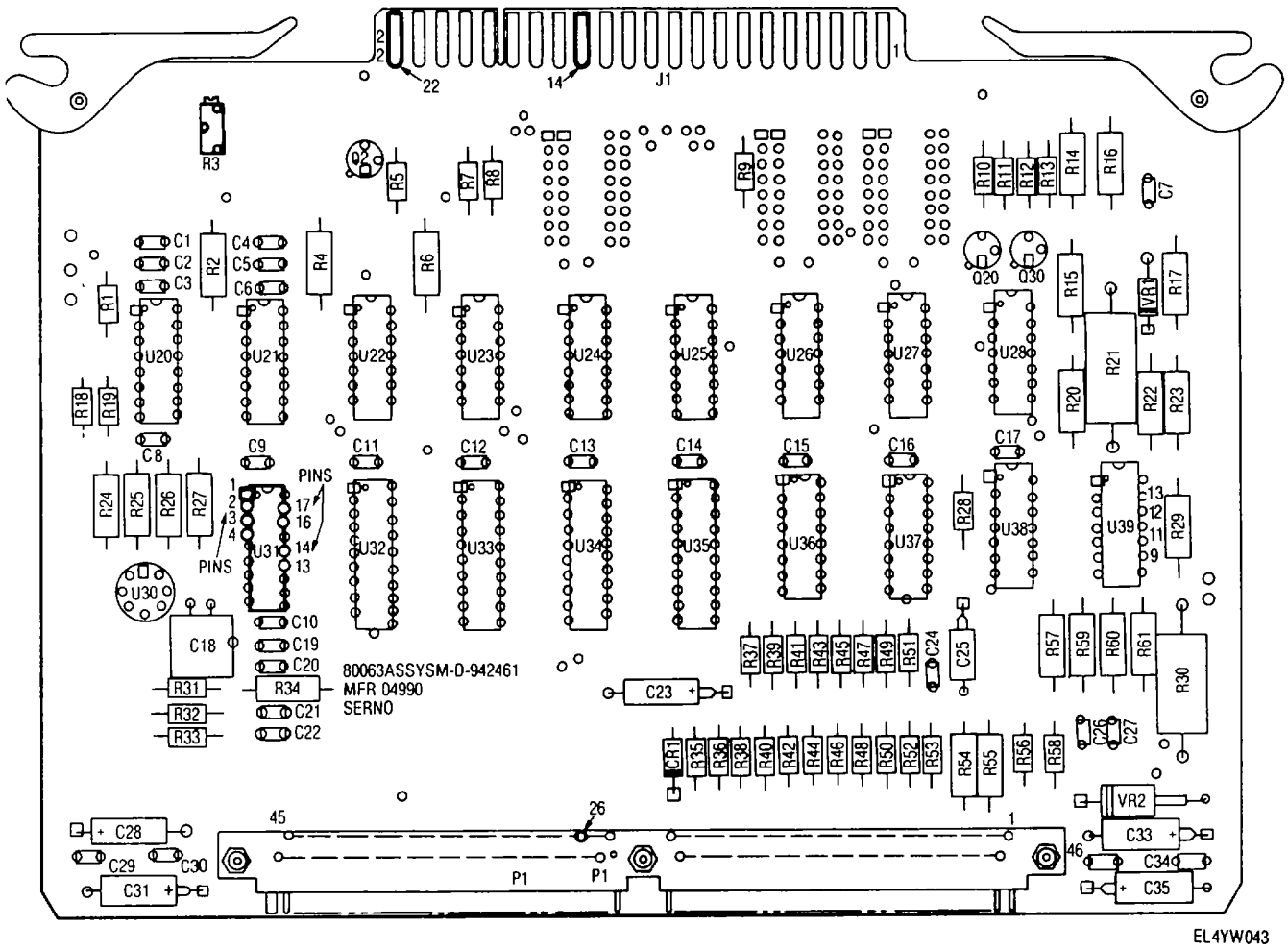


Figure 3-14. Power fault detector 2A13 test point locations.

(23) Adjust oscilloscope for auto trigger, 2 V/division vertical, and 10 microseconds/division horizontal.

(24) Using channel A of oscilloscope, probe pins 1, 2, 3, 4, 13, 14, 16, and 17 of U31 for digital activity

NOTE

The signals on the pms of U31 are irregular. Ensure that both logic levels occur. A logic "1" is defined as between + 2.4V and + 5 OV A logic "0" is defined as between O.OV and + 0.4V

(25) Remove the probe tip from the circuit card test point and set the POWER switches on the equipment to their off positions Remove the circuit card under test and the program card from the test setup.

3-35. Testing Output Memory 2A14

a. Test Setup Connect the equipment as shown in figure 3-10

b. Preliminary Control Settings Prior to testing the circuit card, set the equipment controls as follows

Control	*Setting*
Control interface unit	
POWER ON/OFF	OFF
MODE SELECT	POWER OFF
Digital tester	
POWER	Down (off)
UUT POWER	Down (off)
TEST RATE PER SEC	400K
NUMBER OF TESTS	1M
DISPLAY	PASS/FAIL
PROBE THRESHOLD	2V

c. Test Procedure. Perform the following steps in the sequence given. Change equipment control settings only when instructed in the test procedure

(1) Verify that cable W3 is connected as shown in figure 3-10 and insert the circuit card to be tested into the MODULE TEST circuit card rack connector J1 on the control interface unit.

(2) Insert A14 program card no 1 (SM-A-942370-1) into the card reader slot on the digital tester

(3) On the control interface unit, set the POWER

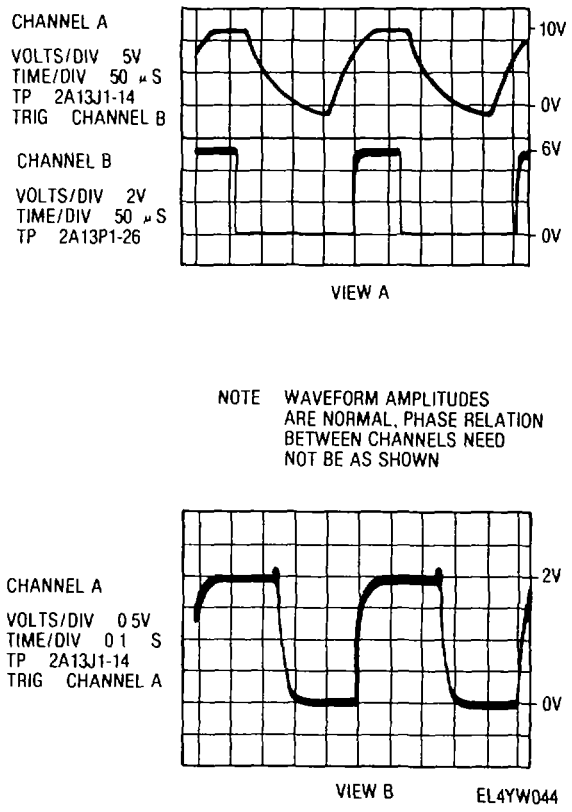


Figure 3-15. Power fault detector 2A13 waveforms

ON/OFF switch to ON and the MODE SELECT switch to MODULE TEST ENC Verify that the MODE/POWER MODULE TEST ON green indicator lamp is illuminated

NOTE

The MODE/POWER SHORT red indicator lamp will be illuminated at this time, but will be extinguished when the digital tester UUT POWER switch is set to the ON position in the following step

(4) On the digital tester, set the POWER and UUT POWER switches to the on positions (up). Verify that the red indicator lamps for these switches are illuminated and the MODE/POWER SHORT lamp is off.

(5) On the digital tester, load the program on the A14 program card no 1 into the digital tester memory by pressing the PROGRAM ENTER momentary switch to the down position

NOTE

The PROGRAM ENTER red indicator lamp will be illuminated during the program enter period

(6) Verify that the READY/ERROR white indicator lamp on the digital tester illuminates when the program has been entered.

(7) Initiate a complete test sequence by pressing either one of the TEST momentary switches to the down position.

NOTE

The TEST red indicator lamp for the switch selected will be illuminated while the test is m progress

(8) Initiate a second test by repeating step (7) above Verify that the green PASS indicator lamp on the digital tester illuminates at the completion of the second test

(9) Set the DISPLAY switch on the digital tester to PROBE.

(10) Refer to figure 3-16 for test point locations and connect the logic probe to each test point listed below. While monitoring each test point, initiate a test by pressing down on the digital tester TEST switch. Verify that the correct corresponding transition counts are displayed on the digital tester counter

Test Point	Count
U27-2	2918
U27-3	2918
U27-4	23535

(11) Connect the logic probe to each test point listed below While monitoring each test point, initiate a test by pressing down on the digital tester TEST switch Verify that the logic probe tip is illuminated or off during the test as shown below

Test Point	*Probe Tip*
U39-12	Illuminated
U39-13	Illuminated
U28-11	Illuminated
U28-9	Off

(12) Set the DISPLAY switch on the digital tester to PASS/FAIL

(13) Remove A14 program card no 1 from the card reader slot

(14) Insert A14 program card no. 2 (SM-A-942370-2) into the card reader slot

(15) On the digital tester, load the program on the A14 program card no 2 into the digital tester memory by pressing the PROGRAM ENTER momentary switch to the down position

(16) Verify that the READY/ERROR white indicator lamp on the digital tester illuminates when the program has been entered

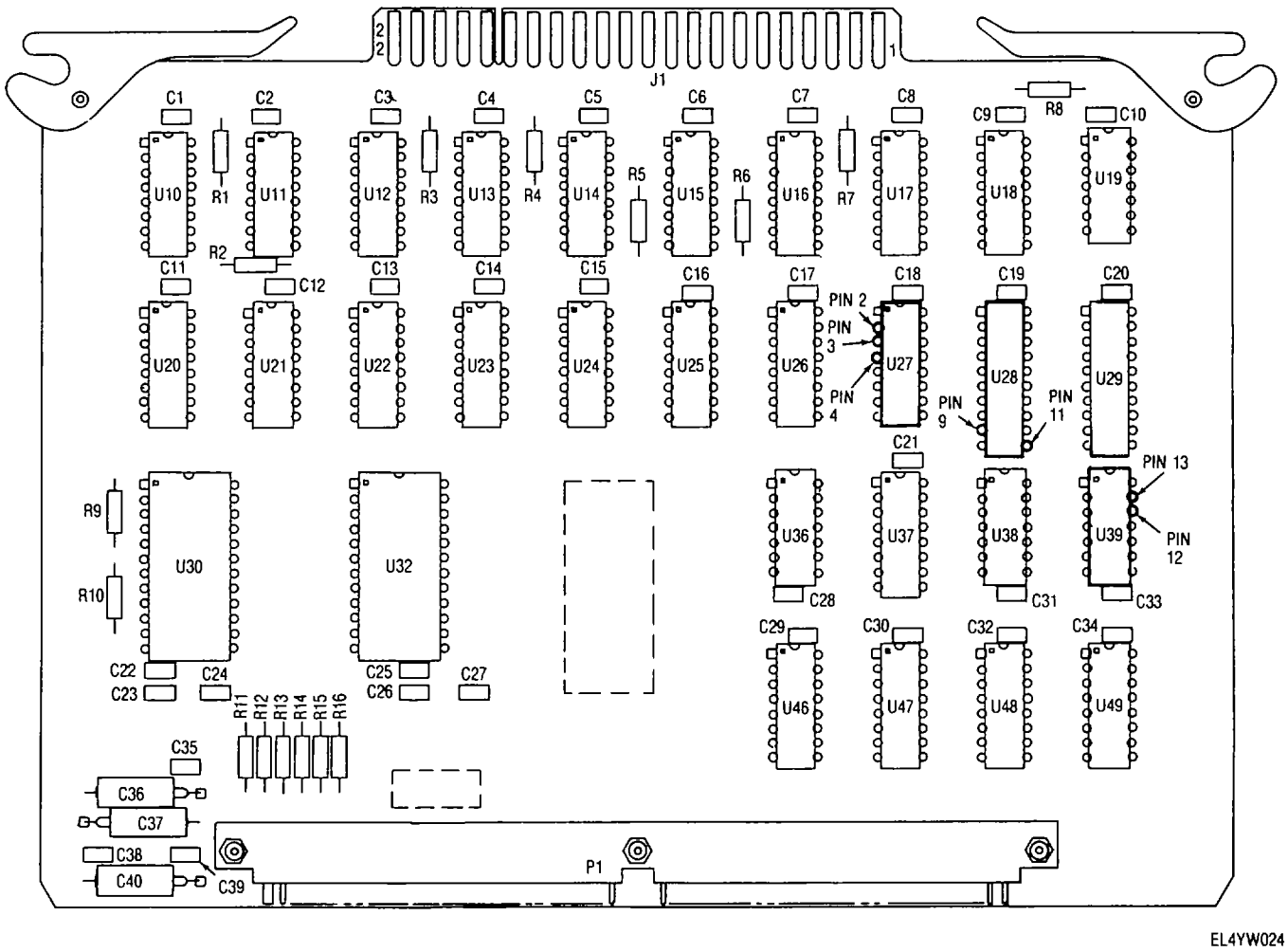
(17) Inflate a complete test sequence by pressing either one of the TEST momentary switches to the down position

(18) Initiate a second test by repeating step (17) above. Verify that the green PASS indicator lamp on the digital tester illuminates at the completion of this second test

(19) Set the POWER switches on the equipment to their off positions Remove the circuit card under test and the program card from the test setup.

3-36. Testing ADAS Control 2A16

a. Test Setup. Connect the equipment as shown in figure 3-10.



EL4YW024

Figure 3-16. Output memory 2A14 test point locations.

b. Preliminary Control Settings. Prior to testing the circuit card, set the equipment controls as follows.

Control	*Setting*
Control interface	
POWER *ON/OFF*	OFF
MODE SELECT	POWER OFF
Digital tester	
POWER	Down (off)
UUT POWER	Down (off)
TEST RATE PER SEC	1M
NUMBER OF TESTS	2M
DISPLAY	PASS/FAIL
PROBETHRESHOLD	2V

c. Test Procedure Perform the following steps in the sequence given. Change equipment control settings only when instructed in the test procedure

(1) Verify that cable W3 is connected as shown in figure 3-10 and insert the circuit card to be tested into the MODULE TEST circuit card rack connector J1 on the control interface unit.

(2) Insert A16 program card no. 1 (SM-A-942450-1) into the card reader slot on the digital tester

(3) On the control interface unit, set the POWER ON/OFF switch to ON and the MODE SELECT switch to MODULE TEST ENC Verify that the MODE/POWER MODULE TEST ON green indicator lamp is illuminated.

NOTE

The MODE/POWER SHORT red indicator lamp will be illuminated at this time, but will be extinguished when the digital tester UUT POWER switch is set to the ON position m the following step.

(4) On the digital tester, set the POWER and UUT POWER switches to the on positions (up). Verify that the red indicator lamps for these switches are illuminated and the MODE/POWER SHORT lamp is off.

(5) On the digital tester, load the program on the A16 program card no. 1 into the digital tester memory by pressing the PROGRAM ENTER momentary switch to the down position

NOTE

The PROGRAM ENTER red indicator lamp

will be illuminated during the program enter period

(6) Verify that the READY/ERROR white indicator lamp on the digital tester illuminates when the program has been entered.

(7) Initiate a complete test sequence by pressing either one of the TEST momentary switches to the down position.

NOTE

The TEST red indicator lamp for the switch selected will be illuminated while the test is in progress.

(8) Initiate a second test by repeating step (7) above. Verify that the green PASS indicator lamp on the digital tester illuminates at the completion of the second test.

(9) Remove A16 program card no. 1 from the card reader slot on the digital tester

(10) Insert A16 program card no 2 (SM-A-942450-2) into the card reader slot.

(11) On the digital tester, load the program on the A16 program card no 2 into the digital tester memory by pressing the PROGRAM ENTER momentary switch to the down position.

(12) Verify that the READY/ERROR white indicator lamp on the digital tester illuminates when the program has been entered

(13) Initiate a complete test sequence by pressing either one of the TEST momentary switches to the down position.

(14) Initiate a second test by repeating step (13) above. Verify that the green PASS indicator lamp on the digital tester illuminates at the completion of this second test.

(15) Remove A16 program card no 2 from the card reader slot on the digital tester

(16) Insert A16 program card no. 3 (SM-A-942450-3) into the card reader slot.

(17) On the digital tester, load the program on the A16 program card no 3 into the digital tester memory by pressing the PROGRAM ENTER switch to the down position

(18) Verify that the READY/ERROR white indicator lamp on the digital tester illuminates when the program has been entered.

(19) Initiate a complete test sequence by pressing either one of the TEST switches to the down position.

(20) Initiate a second test by repeating step (19) above Verify that the green PASS indicator lamp on the digital tester illuminates at the completion of this test.

(21) Remove A16 program card no. 3 from the card reader slot in the digital tester

(22) Insert A16 program card no 4 (SM-A-942450-4) into the card reader slot

(23) On the digital tester, load the program on the A16 program card no. 4 into the digital tester memory by pressing the PROGRAM ENTER switch to the down position

(24) Verify that the READY/ERROR white indicator lamp on the digital tester illuminates when the program has been entered.

(25) Initiate a complete test sequence by pressing either one of the TEST switches to the down position.

(26) Initiate a second test by repeating step (25) above. Verify that the green PASS indicator lamp Illuminates at the completion of this test.

(27) Remove A16 program card no. 4 from the card reader slot on the digital tester

(28) Insert A16 program card no. 5 (SM-A-942450-5) into the card reader slot.

(29) On the digital tester, load the program on the A16 program card no 5 into the digital tester memory by pressing the PROGRAM ENTER switch to the down position

(30) Verify that the READY/ERROR white indicator lamp on the digital tester illuminates when the program has been entered

(31) Initiate a complete test sequence by pressing either one of the TEST switches to the down position

(32) Initiate a second test by repeating step (31) above. Verify that the green PASS indicator lamp illuminates at the completion of this test

(33) Set the POWER switches on the equipment to their off positions. Remove the circuit card under test and the program card from the test setup

3-37. Testing Video Interface 2A17

a. Test Setup. Connect the equipment as shown in figure 3-8.

b. Preliminary Control Settings Prior to testing the circuit card, set the equipment controls as follows

Control	*Setting*
Control interface unit	
POWER ON/OFF	OFF
MODE SELECT	POWER OFF
Digital tester	
POWER	Down (off)
UUT POWER	Down (off)
TEST RATE PER SEC	2M
NUMBER OF TESTS	2M
DISPLAY	PASS/FAIL
PROBE THRESHOLD	2V

c. Test Procedure. Perform the following steps in the sequence given. Change equipment control settings only when instructed in the test procedure

(1) Insert the circuit card to be tested into the MODULE TEST circuit card rack connector J1 on the control interface unit.

(2) Insert A17 program card no. 1 (SM-A-942440-1) into the card reader slot on the digital tester.

(3) On the control interface unit, set the POWER

ON/OFF switch to ON and the MODE SELECT switch to MODULE TEST ENC Verify that the MODE/POWER MODULE TEST ON green indicator lamp is illuminated.

NOTE

The MODE/POWER SHORT red indicator lamp will be illuminated at this time, but will be extinguished when the digital tester UUT POWER switch is set to the ON position in the following step.

(4) On the digital tester, set the POWER and UUT POWER switches to the on positions (up). Verify that the red indicator lamps for these swatches are illuminated and the MODE/POWER SHORT lamp is off.

(5) On the digital tester, load the program on the A17 program card no. 1 into the digital tester memory by pressing the PROGRAM ENTER momentary switch to the down position

NOTE

The PROGRAM ENTER red indicator lamp will be illuminated during the program enter period.

(6) Verify that the READY/ERROR white indicator lamp on the digital tester illuminates when the program has been entered.

(7) Refer to figure 3-17 for test point locations and connect channel A of the oscilloscope between test points J1-P and J1-22 (gnd).

(8) Connect channel B of the oscilloscope between test points J1-N and J1-22 (gnd)

(9) Depress CONT TEST switch on the digital tester. Verify that the display on channels A and B of the oscilloscope is similar to that shown in view A of figure 3-18.

(10) Connect channel A of the oscilloscope between test points J1-17 and J1-22 (gnd).

(11) Connect channel B of the oscilloscope between test points J1-S and J1-22 (gnd)

(12) Verify that the display on channels A and B is similar to that shown m view B of figure 3-18

(13) Remove A17 program card no. 1 from the card reader slot on the digital tester.

(14) Insert A17 program card no 2 (SM-A-942440-2) into the card reader slot

(15) On the digital tester, load the program on the A17 program card no. 2 into the digital tester memory by pressing the PROGRAM ENTER momentary switch to the down position.

(16) Verify that the READY/ERROR white indicator lamp on the digital tester illuminates when the program has been entered

(17) Depress the CONT TEST switch on the digital tester and verify that the display on channels A and B is similar to that shown in view C of figure 3-18

(18) Connect channel A of the oscilloscope between test points J1-F and J1-22 (gnd).

(19) Connect channel B of the oscilloscope between test points J1-D and J1-22 (gnd)

(20) Verify that the display on channels A and B of the oscilloscope is similar to that shown in view D of figure 3-18

(21) Remove A17 program card no 2 from the card reader slot on the digital tester

(22) Insert A17 program card no 3 (SM-A-942440-3) into the card reader slot

(23) On the digital tester load the program on the A17 program card no 3 into the digital tester memory by pressing the PROGRAM ENTER switch to the down position

(24) Verify that the READY/ERROR white indicator lamp on the digital tester illuminates when the program has been entered.

(25) Depress the CONT TEST switch on the digital tester

(26) Using the DVM for indication, adjust power supply PP-3940/G for + 1.0 + 0.1 volt.

(27) Connect the negative lead of the power supply to test point J1-22 (gnd) and the positive lead to test point P1-14.

(28) Connect the positive lead of the DVM to test point J1-N and the negative lead to J1-22.

(29) Verify that the indication on the DVM is greater than + 2.5 volts

(30) Reverse the leads of the power supply so that a negative voltage will be applied to P1-14.

(31) Verify that the DVM indication is less than + 0 4 volt.

(32) Remove the power supply leads from the circuit card under test and adjust the power supply voltage for +2 0 volts. If the leads were reversed at the power supply (step 30, above), return them to the proper outputs

(33) Connect the negative lead of the power supply to test point P1-7 and the positive lead to J1-22.

(34) Connect the DVM between test points J1-D and J1-22 (gnd).

(35) Verify that the DVM indication is greater than + 2 5 volts.

(36) Remove the power supply leads from the **cir**cuit card under test

(37) Set the POWER switches on the equipment to their off positions Remove the circuit card under
test and the program card from the test setup

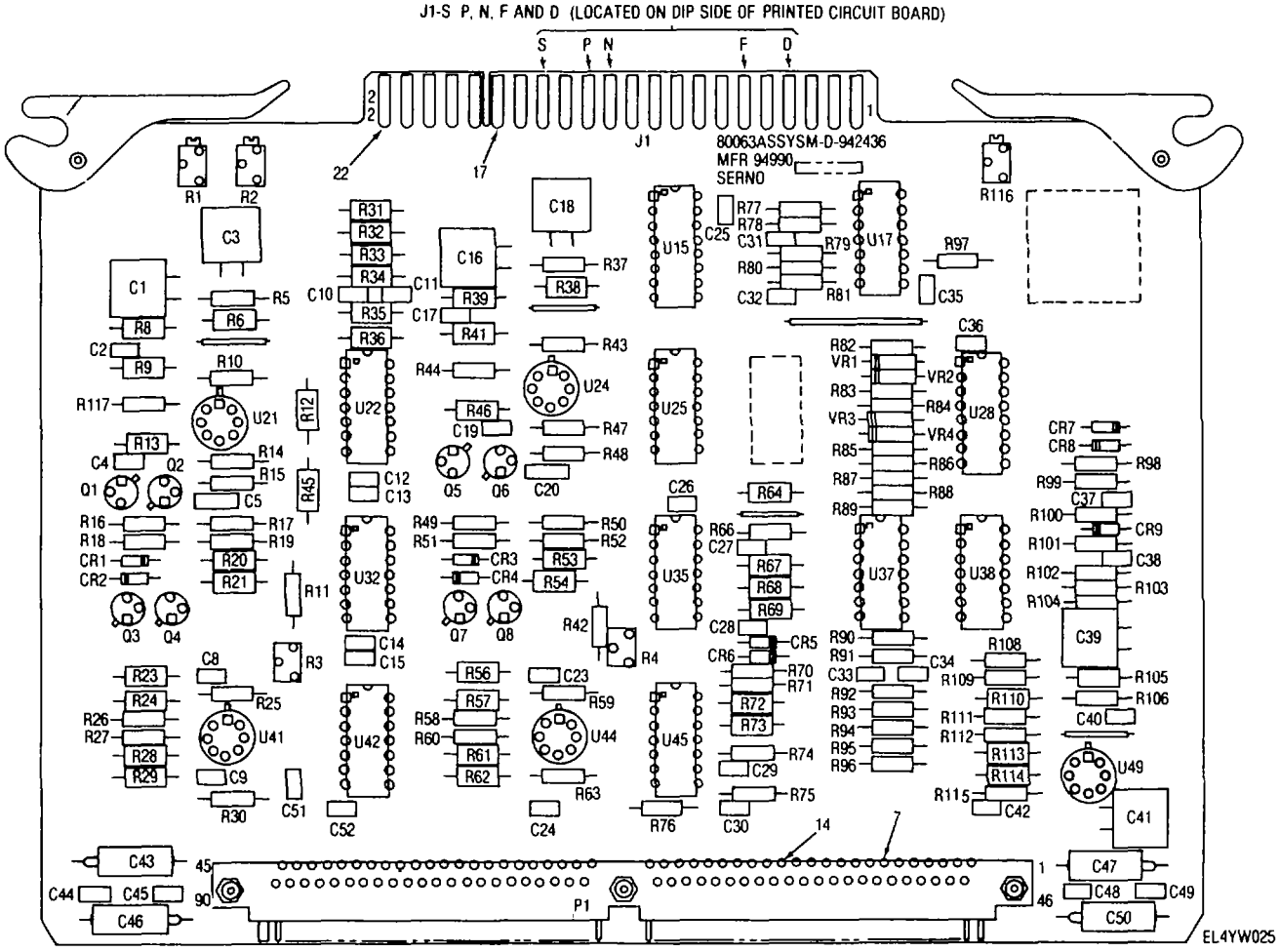


Figure 3-17. Video Interface 2A17 test point locations

Section VI. WIRE LISTS

3-38. General

Wire lists for the encoder and data link control are contained in this section. These wire lists will enable direct support maintenance personnel to perform continuity and resistance measurements to isolate a defective wire path or cable assembly. The interconnection cabling diagram for the data transmitting set is shown in figure 3-19.

3-39. Arrangement of Wire Lists

The wire lists included in this section are listed below

Wire list	*Reference*
Encoder	Table 3-8
Electrical filter assembly 2FL1	Table 3-9
Data link control	Table 3-10

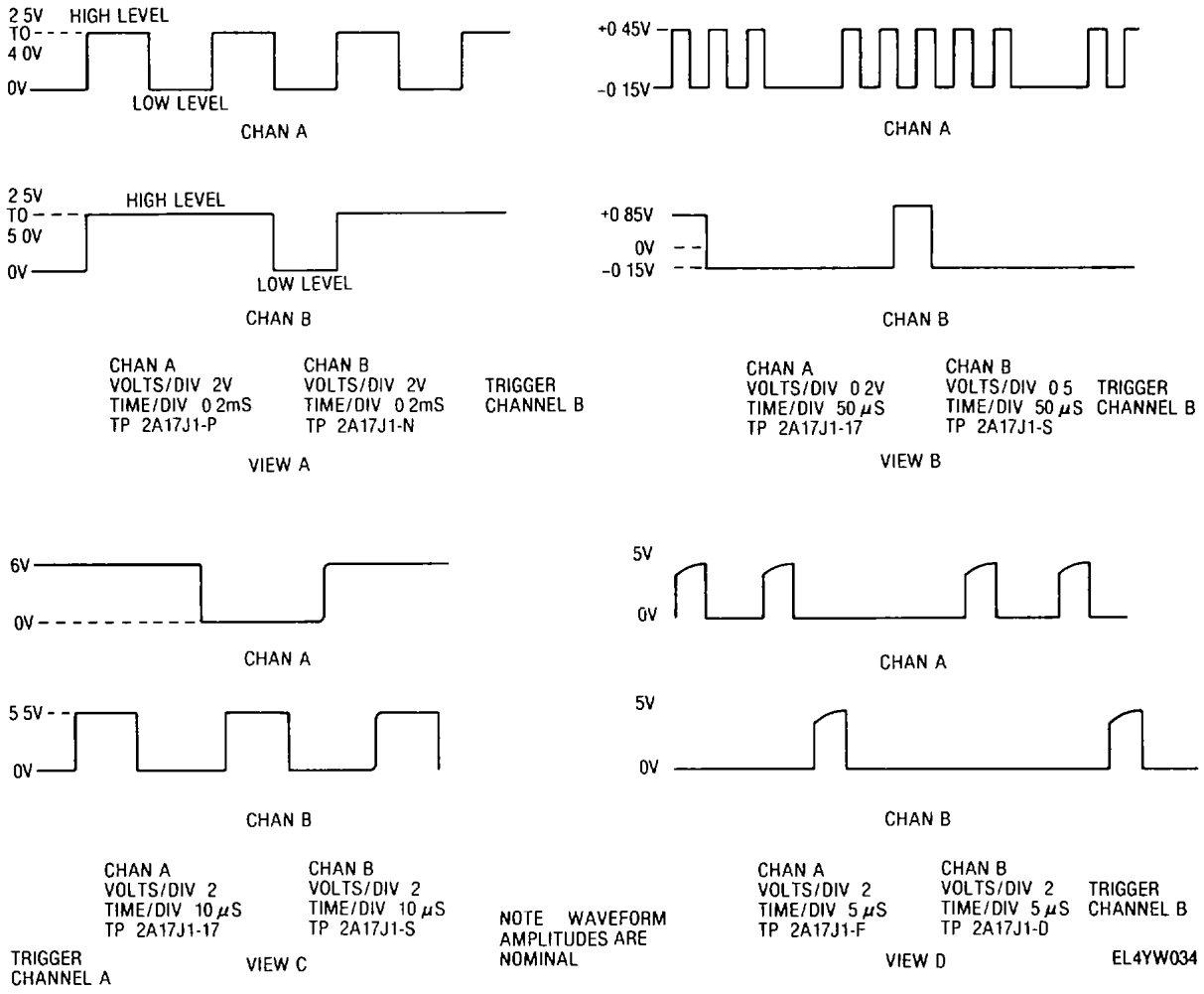


Figure 3-18. Video interface 2A17 waveforms

Table 3-8. Encoder Wire List

Wire no.	From	To	Color	Size (A *WG*)	Remarks
1	J1-A	K1-X2	RED	20	
2	J1-B	P2-27	BLK	20	
3	J1-C	E1B	BLK	20	
4	J1-D	P2-11	WHT	20	
5	J1-F	P2-3	RED	20	
6	J1-H	P2-15	WHT	20	
7	J1-K	P1-16	WHT	20	
8	J1-M	J4-P	WHT	20	
9	J1-N	P1-32	WHT	20	
10	J1-R	P1-35	WHT	20	
11	J1-T	PI-19	WHT	20	
12	J1-U	P2-2	WHT	20	
13	J3-A	E1B	BLK	20	
14	J3-C	P1-48	WHT	20	
15	J3-D	P2-34	WHT	20	
16	J3-E	PI-49	WHT	20	
17	J3-F	P2-17	WHT	20	
18	J3-G	P2-33	WHT	20	
19	J3-H	P2-28	WHT	20	
20	J3-J	P2-31	WHT	20	

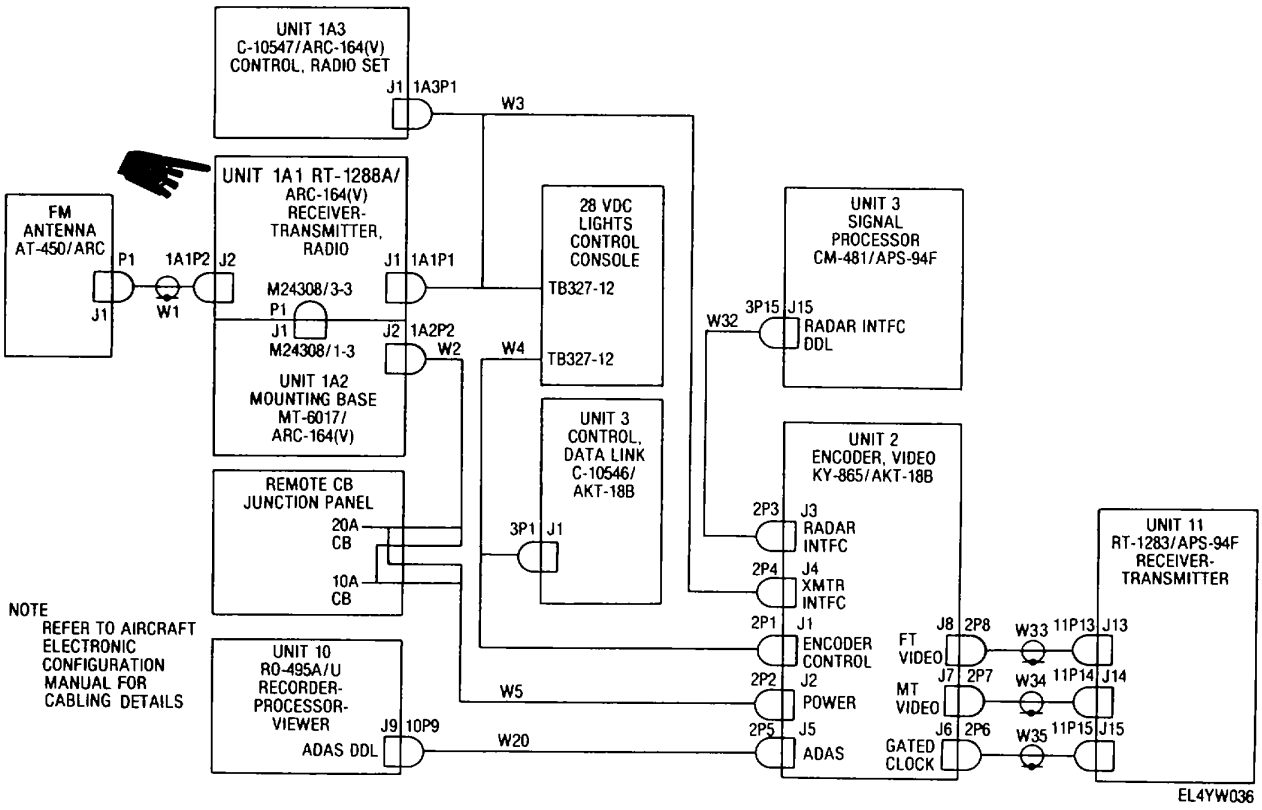


Figure 3-19. Data transmitting set cabling diagram.

Table 3-8. Encoder Wire List-Continued

Wire no.	*From*	To	*Color*	*Size (A WG)*	*Remarks*
21	J3-K	P2-35	WHT	20	
22	J3-V	P2-21	WHT	20	
23A	J4-A	E1B	BLK	20	
23B	J4-A	J4-W SHLD	BLK	20	
24	J4-C	P2-16	*WHT*	20	
25	J4-E	P2- 12	WHT	20	
26	J4-J	Pl-10	RED	20	
27A	J4-W	P2-8	WHTSHLD	22	
27B	J4-WSHLD	J4-Z SHLD	BLK	20	
27C	P2-8 SHLD	P2-26	BLK	20	
28A	J4-Z	P2-25	WHTSHLD	22	
28B	P2-25 SHLD	P2-7	BLK	20	
29A	J5-A	P1-26	WHTSHLD	22	
29B	J5A SHLD	J5-B	BLK	20	
29C	P1-26SHLD	P1-43	BLK	20	
30	J5-G	P2-4	WHT	20	
31	J5-H	P2-5	WHT	20	
32	J5-L	E1B	WHT	20	
33A	J5-M	P1-24	WHTSHLD	22	
33B	J5-M SHLD	J5-U SHLD	BLK	20	
33C	P1-24SHLD	P1-25	BLK	20	
34	J5-N	E1B	BLK	20	
35A	J5-U	P1-41	WHTSHLD	22	
35B	J5-U SHLD	J5-V SHLD	BLK	20	
35C	P1-41 SHLD	P1-42	BLK	20	
36A	J5-V	P1-5	WHTSHLD	22	
36B	J5-V SHLD	J5-W SHLD	BLK	20	

Table 3-8. Encoder Wire List-Continued

Wire no	*From*	To	Color	*Size (A WG)*	*Remarks*
36C	P1-5 SHLD	P1-6	BLK	20	
37A	J5-W	P1-21	WHTSHLD	22	
37B	J5-W SHLD	J5-X SHLD	BLK	20	
37C	P1-21 SHLD	P1-22	BLK	20	
38A	J5-X	P2-28	WHT SHLD	22	
38B	J5-X SHLD	J5-Y	BLK	20	
38C	P2-28 SHLD	P2-29	BLK	20	
39A	J6	P1-40RG-180 BU			
39B	J6 SHLD	E12	BLK	20	
39C	P1-40SHLD	Pl-23	BLK	20	
40A	**J7**	P1-47RG-180 *BIU*			
40B	J7 SHLD	E13	BLK	20	
40C	P1-47 SHLD	P1-30	BLK	20	
41A	J8	Pi-29RG-180 E/U			
41B	J8SHLD	E14	BLK	20	
41C	P1-29 SHLD	P1-44	BLK	20	
42	Pl-2	E1A	BLK	20	
43	P1-37	K1-X2	RED	20	
44	P2-19	E7	BLU	20	
45	P2-22	Kl-Xl	RED	20	
46	P3-A1	U2-	GRN	16	
47	P3-A2	E4	GRN	16	
48	P3-A3	PS1-3	YEL	16	
49	P3-A4	PS1-3	YEL	16	
50	P3-A5	ElA	BLK	16	
51	P3-A6	E1A	BLK	16	
52	P3-A7	E1A	BLK	16	
53	P3-A8	E1A	BLK	16	
54	P4-1	ElA	BLK	20	
55	P4-2	ElA	BLK	20	
56	P4-3	K1-B2	GRAY	20	
57	P4-4	K1-B2	GRAY	20	
58	P4-5	K1-A2	GRAY	20	
59	P4-6	K1-A2	GRAY	20	
60	P4-7	E1A	BLK	20	
61	P4-8	Kl-Xl	RED	20	
62	PSi-i	PS2-1	GRAY	20	
63	PSi-i	Ell	GRAY	16	
64	PS1-2	E10	GRAY	16	
65	PS1-2	PS2-2	GRAY	20	
66	PS1-3	E2	YEL	16	
67	PS1-4	E1-A	BLK	16	
68	PSi-4	E3	BLK	16	
69	PS1-4	El-A	BLK	16	
70	PS2-1	PS3-1	GRAY	16	
71	PS2-2	PS3-2	GRAY	16	
72	PS2-3	U2-	BLK	16	
73	PS2-4	U2+	GRN	16	
74	PS3-3	E4	ORN	16	
75	PS3-4	E5	BLK	16	
76	PS3-5	E7	BLUE	20	
77	Bl-Tl	E10	GRAY	16	
78	B1-T4	E9	GRAY	16	
79	B1-T8	ES	GRAY	16	
80	Mi-l	Ell	GRAY	20	
81	M1-2	E10	GRAY	20	
82	U2+	ElA	BLK	16	
83	K1-Al	Ell	GRAY	16	
84	Kl-Bl	EO10	GRAY	16	
87	E6	ElA	BLK	16	
88	E5	E6	BLK	16	
89	E9	Ell	GRAY	16	

Table 3-8. Encoder Wire List-Continued

Wire no	From	To	*Color*	*Size(AWG)*	Remarks
91	P1-1			20	SPARE
92	P1-3			20	SPARE
93	P1-4			20	SPARE
94	P1-7			20	SPARE
95	P1-8			20	SPARE
96	P1-9			20	SPARE
97	P1-ll			20	SPARE
98	P1-12			20	SPARE
99	Pl-13			20	SPARE
100	P1-14			20	SPARE
101	P1-15			20	SPARE
102	P1-17			20	SPARE
103	P1-18			20	SPARE
104	P1-20			20	SPARE
105	P1-27			20	SPARE
106	P1-31			20	SPARE
107	P1-33			20	SPARE
108	P1-34			20	SPARE
109	P1-36			20	SPARE
110	P1-38			20	SPARE
111	P1-39			20	SPARE
112	P1-45			20	SPARE
113	P1-46			20	SPARE
114	P1-50			20	SPARE
115	P2-1			20	SPARE
116	P2-6			20	SPARE
117	P2-9			20	SPARE
118	P2-10			20	SPARE
119	P2-13			20	SPARE
120	P2-14			20	SPARE
121	P2-18			20	SPARE
122	P2-20			20	SPARE
123	P2-23			20	SPARE
124	P2-24			20	SPARE
125	P2-30			20	SPARE
126	P2-32			20	SPARE
127	P2-36			20	SPARE
128	P4-9			20	SPARE

Table 3-9. Electrical Filter Assembly 2FL1 Wire List

Wire no.	*From*	*To*	*Color*	*Size (AWG)*	Remarks
1	J2-D	XF3-1	RED	20	
2	XF3-2	RV1-1			
3	XFL1-2	J1-8	RED	20	
4	J2-E	E3	BLK	20	
5	XFL2-2	J1-7	BLK	20	
6	J2-J	XF1-1	GRAY	16	
7	XF1-2	L1-1	GRAY	16	
8	L1-2	Cl-l	GRAY	16	
9	C1-2	J1-6	GRAY	20	
10	C1-2	J1-5	GRAY	20	
11	J2-L	XF2-1	GRAY	16	
12	XFn-2	L2-1	GRAY	16	
13	L2-2	C2-1	GRAY	16	
14	C2-2	J1-4	GRAY	20	
15	C2-2	J1-3	GRAY	20	
16	J2-B	E2	BLK	20	
17	J2-C	E2	BLK	20	
18	J2-F	E2	BLK	20	
19	J2-G	E2	BLK	20	
20	El	J1-2	BLK	20	
21	El	J1-1	BLK	20	
22	E4	FL1-1	RED	20	
23	XF3-2	D1-2	RED	20	
24	D1-l	E4	RED	20	
25	RV1-2	E3	RED	20	
26	D2-1	E4	RED	20	
27	D2-2	E3	RED	20	

Table 3-10. Data Link Control Wire List

Wire no	From	*To*	*Color*	*Size(A* WG)	*Remarks*
1	J1-V	J2-1	RED	22	
2	J1-F	DS1-1	RED	22	
3	DS1-1	DS2-1	RED	22	
4	DS2-1	DS3-1	RED	22	
5	J1-U	DS3-2	WHT	22	
6	J1-R	DS2-2	WHT	22	
7	J1-T	DS1-2	WHT	22	
8	J1-B	J2-2	BLK	22	
9	J2-2	S3-2	BLK	22	
10	S3-2	S2-2	BLK	22	
11	S2-2	S1A-W	BLK	22	
12	S1A-W	S1B-W	BLK	22	
13	S3-2	J1-M	BLK	22	
14	J1-K	S3-1	WHT	22	
15	J1-N	S2-1	WHT	22	
16	J1-H	S1A-2	WHT	22	
17	J1-D	S1A-3	WHT	22	
18	J1-A	S1B-2	RED	22	
19	S1B-2	S1B-3	RED	22	
20	J1-C	J2-2	BLK	22	

APPENDIX A

REFERENCES

DA Pam 310-1	Consolidated Index of Army Publications and Blank Forms
TB 43-0118	Field Instructions for Painting and Preserving Electronics Command Equipment Including Camouflage Pattern Painting of Electrical Equipment Shelters
TB 385-4	Safety Precautions for Maintenance of Electrical Electronic Equipment
TM 11-1510-204-20-2-1	Organizational Maintenance Manual for Signal Electronic Equipment Configurations, Army Model OV-1D Aircraft (NSN 1510-00-869-3654)
TM 11-5841-286-13	Operator's, Organizational, and Direct Support Maintenance Manual for Radio Set AN/ARC-164(V)12 (NSN 5821-01-071-5624)
TM 11-5841-287-12	Operator's and Organizational Maintenance Manual Transmitting Set, Radar Data AN/AKT-18B (NSN 5841-01-070-4408)
TM 11-6130-247-15	Operator's, Organizational, Direct Support, General Support, and Depot Maintenance Manual (Including Repair Parts and Special Tools List) Power Supply PP-3940/G.
TM 11-6625-444-14-1	Operator's, Organizational, Direct Support and General Support Maintenance Manual Including Repair Parts and Special Tools List. Voltmeter, Digital AN/GSM-64B (NSN 6625-00-022-7894) Including Plug-In, Electronic Test Equipment PL-1370/GSM-64B (NSN 6625-00-137-8366)
TM 11-6625-654-14	Operator's, Organizational, Direct Support and General Support Maintenance Repair Parts and Special Tools List (Including Depot Maintenance Repair Parts and Special Tools List) for Multimeter ANIUSM-223.
TM 11-6625-2658-14	Operator's, Organizational, Direct Support and General Support Maintenance Manual for Oscilloscope ANIUSM-281C (NSN 6625-00-106-9622)
TM 11-6625-2937-13	Operator's, Organizational, and Direct Support Maintenance Manual for Test Set, Electronic Systems AN/UKM-5 (NSN 6625-01-073-9858)
TM 11-6625-2950-13	Operator's, Organizational, and Direct Support Maintenance Manual for Test Set Group, Radio OQ-273/ARC-164(V) (NSN 5821-01-072-8146)
TM 11-6625-2951-13	Operator's, Organizational, and Direct Support Maintenance Manual for Test Set, Electronic Systems AN/UYM-7 (NSN 6625-01-016-1866)
TM 38-750	The Army Maintenance Management System (TAMMS).

APPENDIX B

EXPENDABLE SUPPLIES AND MATERIALS LIST

Section I. INTRODUCTION

B-1. Scope

This appendix lists expendable supplies and materials you will need to operate and maintain the AN/AKT-18B These items are authorized to you by CTA 50-970, Expendable Items (Except Medical, Class V, Repair Parts, and Heraldic Items).

B-2. Explanation of Columns

a. *Column 1-Item Number* This number is assigned to the entry in the listing and is referenced in the narrative instructions to identify the material (e g, "Use Cleaning Compound, item 5, App. D').

b. Column 2-Level. This column identifies the lowest level of maintenance that requires the listed item.

C-Operator/Crew
O-Organizational Maintenance
F-Direct Support Maintenance
H-General Support Maintenance

c. *Column 3-National Stock Number* This is the National stock number assigned to the item, use it to request or requisition the item.

d. Column 4-Descnption Indicates the Federal item name and, if required, a description to identify the item. The last line for each item indicates the part number followed by the Federal Supply Code for Manufacturer (FSCM) in parentheses, if applicable

e. *Column 5-Unit of Measure (U/M)* Indicates the measure used in performing the actual maintenance function This measure is expressed by a two-character alphabetical abbreviation (e g , ea, in, pr) If the unit of measure differs from the unit of issue, requisition the lowest unit of issue that will satisfy your requirements.

(Next printed page is B-2)

SECTION II EXPENDABLE SUPPLIES AND MATERIALS LIST

(1) ITEM NUMBER	(2) LEVEL	(3) NATIONAL STOCK NUMBER	(4) DESCRIPTION PART NUMBER AND FSCM	(5) UNIT OF MEAS
1	F	8020-00-257-0382	BRUSH, ARTIST	EA
2	F	8030-00-962-4432	COMPOUND, CONDUCTIVE EPOXY	TB
3	F	8010-00-297-0547	COMPOUND, HEATSINK, DC-340 (71984)	TB
4	F		ENAMEL, LUSTERLESS BLACK,	CN
5	F	8010-00-297-2097	ENAMEL, LUSTERLESS GRAY	CN
6	F	8010-00-297-0560	ENAMEL, LUSTERLESS OLIVE DRAB	GL
7	F	8010-00-835-2114	PRIMER, ZINC, CHROMATE, MIL-P-8585	PT
8	F	5350-00-264-3485	SANDPAPER, FINE	PK
9	F	3439-00-194-9727	SOLDER (81349)	LB
10	F	3439-00-824-9856	SOLDER, SN60 WRAP 30 0-32 (81349)	LB
11	F		SOLDER BRAID, CAT #40-3-5, SIZE 3 (34605)	PK
12	F	6850-00-105-3084	TRICHLOROTRIFLUOROETHANE, FREON, TYPE TF	CN

GLOSSARY

$\phi 2$, $\overline{\phi 2}$	Internal MPU clock
OXXX	Used for bus control during ROM operations, OXXX is TRUE when addresses A13, A14, and A15 are low
	A
A0 to A15	Individual microprocessor address bits.
ADAS	Airborne Data Annotation System
ADAS CLOCK	Clock used to synchronize the transfer of ADAS data
ADAS DISABLE	Disables transfer of accumulated video while ADAS data is being received.
ADAS IRF	ADAS interface.
ADAS RDY	ADAS data word ready-one of four basic interrupts
ADLE	Timing for analog-to-digital output latch-even range bins.
ADLO	Timing for analog-to-digital output latch-odd range bins
ANTENNA SELECT	External signal signifying from which side the SLAR antenna is looking.
ANT XTN DET	Antenna transition detector-determines when SLAR is using both antenna mode
	B
BA	MPU disabled-address bus available
B/C	B versus C field video
BCD MODE	Binary coded decimal mode-ADAS can be either BCD or numeric data
B-FT	BITE FT-generates fixed target video during BITE
B GTD 5 MHz	BITE gated 5 MHz-internally generated range bin clock
BITE	Built-in test equipment.
BITE LITE	Turns on BITE IN PROCESS lamp during BITE test
B-MT	BITE MT-generates moving target video during BITE
BOTH ANT	Video data processing **is** in both antenna mode
BTR RES	Resets BITE request latches
	C
CLEAR	Drift angle data ready-one of four basic interrupts.
28V CONT POWR	Control power signal used to enable primary power relay K1
	D
DO to D7	Microprocessor data bus bits 0 through 7
DLY (0-50)	Video delay information from SLAR
DRIFT ANG	Drift angle
	E
EN BIPL	Enables BITE IN PROCESS indicator.
ENCDR ERROR	Enables ENCODER ERROR indicator.
ENCODER	Indicator
ENCODER FAULT	Indicator
	F
FILM SPD	Film speed
FT	Fixed target.
FTO to FT4	Data bit representing FT video (FT4 is most significant)
FT DAINLAR	FT data input latch reset

GLOSSARY-Continued

	G
GTD CLOCK	Gated clock
	H
HALT, HALT	Signal disables microprocessor for use of DATA BUS by video data processing
Hamming code bits	Three error correcting bits
	I
ID	Identifies data as FT or MT video
INT RES	Resets video processing circuits
IWC	Integrated write control signal used to transfer accumulated video into output memory.
	J
	K
	L
LOAD	Initializes video control circuits and range bin address counters
L/R	6 Hz BITE signal which simulates both antenna operation
	M
M10	Most significant address bit on the output memory board
MPU	Microprocessor unit
MT	Moving target
MT DAINLAR	Moving target data Input latch reset
	N
NMI	Nonmaskable interrupt sequence initiated
	O
OUTBUF IRQ	Output buffer interrupt request sequence initiated
OUTPUTIRECV IRF	Output or receive register fault
	P
P	Parity.
PF ERROR	Power fault error signal to enable ENCODER FAULT indicator
PRI	Pulse repetition intervals.
	Q
	R
RAO to RA10	Range bin address 0 through 10
RAOE to RA1OE	Range bin address 0 through 10 even
RAOO to RA10O	Range bin address 0 through 10 odd
RANGE	Kilometers of displayed radar video.
RANGE DELAY	Kilometers of video not shown from aircraft to first video shown
RC	Read control.
R CLEAR	Range bin clear signal to initialize video accumulation.
RCVR	Receive mode of receiver/transmitter operation
RESET	Master reset line-power-on-reset
RESET XTN DET	Initializes antenna transition detector
RT DATA ERROR	One of the four basic interrupts
R/T FAULT	Indicator

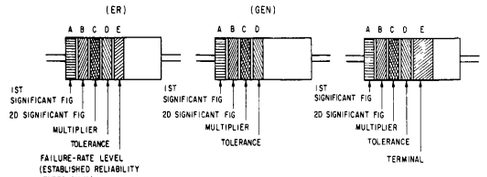
GLOSSARY-Continued

R/T LITE	Signal to enable R/T FAULT indicator
RT MALF	Receiver/transmitter malfunction
RT PWR ON/OFF	Enables RT power on.
R/W (O/E)	Read/write (odd/even) control signal for video accumulation
R/W	MPU is either reading or writing data.
	S
SLAR	Side looking airborne radar
STADC	Start analog-to-digital conversion
STBY	Receiver/transmitter in receive (warmup) mode
STE	Special test equipment
STE CLK	5 MHz STE clock signal
STE CLK SEL	Enables selection of STE CLK instead of on-board clock
STE RESET	Reset initiated by STE
	T
TEST ENC	Testing encoder circuits which modulate fm radio.
	U
	V
VERT SWP	Aircraft drift angle input data.
VID "A"	A-field video fault
VID "B"	B-field video fault
VID BA	Video bus available and microprocessor has halted
VID "C"	V-field video fault.
VMA	Valued memory address present on address bus
	W
WC	Write control from microprocessor
	X
X	Signifies signal X 1is TRUE when low
XMIT REG	Transmit register empty-one of four basic interrupts
XMT	RT operating in transmit mode
XTAL	4 MHz basic clock
	Y
	Z

INDEX

INDEX-continued

U S GOVERNMENT PRINTING OFFICE 1983-664 01511189



COLOR CODE MARKING FOR COMPOSITION TYPE RESISTORS

COLOR-CODE MARKING FOR FILM-TYPE RESISTORS

TABLE I
COLOR CODE FOR COMPOSITION TYPE AND FILM TYPE RESISTORS

BAND A		BAND B		BAND C		BAND D		BAND E		
COLOR	FIRST SIGNIFICANT FIGURE	COLOR	SECOND SIGNIFICANT FIGURE	COLOR	MULTIPLIER	COLOR	RESISTANCE TOLERANCE (PERCENT)	COLOR	FAILURE RATE LEVEL	TERM
BLACK	0	BLACK	0	BLACK	1			BROWN	M=1.0	
BROWN	1	BROWN	1	BROWN	10			RED	P=0.1	
RED	2	RED	2	RED	100			ORANGE	R=0.01	
ORANGE	3	ORANGE	3	ORANGE	1,000			YELLOW	S=0.001	
YELLOW	4	YELLOW	4	YELLOW	10,000	SILVER	±10 (COMP. TYPE ONLY)	WHITE		SOLDERABLE
GREEN	5	GREEN	5	GREEN	100,000	GOLD	±5			
BLUE	6	BLUE	6	BLUE	1,000,000	RED	±2 (NOT APPLICABLE TO ESTABLISHED RELIABILITY)			
PURPLE (VIOLET)	7	PURPLE (VIOLET)	7							
GRAY	8	GRAY	8	SILVER	0.01					
WHITE	9	WHITE	9	GOLD	0.1					

BAND A — THE FIRST SIGNIFICANT FIGURE OF THE RESISTANCE VALUE (BANDS A THRU D SHALL BE OF EQUAL WIDTH)

BAND B — THE SECOND SIGNIFICANT FIGURE OF THE RESISTANCE VALUE

BAND C — THE MULTIPLIER (THE MULTIPLIER IS THE FACTOR BY WHICH THE TWO SIGNIFICANT FIGURES ARE MULTIPLIED TO YIELD THE NOMINAL RESISTANCE VALUE.)

BAND D — THE RESISTANCE TOLERANCE

BAND E — WHEN USED ON COMPOSITION RESISTORS, BAND E INDICATES ESTABLISHED RELIABILITY FAILURE-RATE LEVEL (PERCENT FAILURE PER 1,000 HOURS). ON FILM RESISTORS, THIS BAND SHALL BE APPROXIMATELY 1-1/2 TIMES THE WIDTH OF OTHER BANDS AND INDICATES TYPE OF TERMINAL

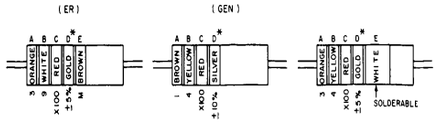
RESISTANCES IDENTIFIED BY NUMBERS AND LETTERS (THESE ARE NOT COLOR CODED)

SOME RESISTORS ARE IDENTIFIED BY THREE OR FOUR DIGIT ALPHA NUMERIC DESIGNATORS. THE LETTER R IS USED IN PLACE OF A DECIMAL POINT WHEN FRACTIONAL VALUES OF AN OHM ARE EXPRESSED. FOR EXAMPLE

2R7 = 2.7 OHMS 1DR0 = 10.0 OHMS

FOR WIRE-WOUND-TYPE RESISTORS COLOR CODING IS NOT USED, IDENTIFICATION MARKING IS SPECIFIED IN EACH OF THE APPLICABLE SPECIFICATIONS

EXAMPLES OF COLOR CODING



NOMINAL RESISTANCE 3,900 OHMS
RESISTANCE TOLERANCE ±5%
FAILURE RATE LEVEL M

NOMINAL RESISTANCE 1,400 OHMS
RESISTANCE TOLERANCE ±10%

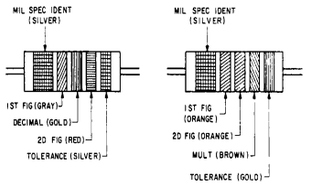
NOMINAL RESISTANCE 3,400 OHMS
RESISTANCE TOLERANCE ±5%
TERMINAL SOLDERABLE

COMPOSITION-TYPE RESISTORS

FILM-TYPE RESISTORS

* IF BAND D IS OMITTED, THE RESISTOR TOLERANCE IS ±20% AND THE RESISTOR IS NOT MIL-STD

A COLOR CODE MARKING FOR MILITARY STANDARD RESISTORS



(A) 82UH ±10%

(B) 330UH ±5%

COLOR CODING FOR TUBULAR ENCAPSULATED R F CHOKES AT A, AN EXAMPLE OF OF THE CODING FOR AN 8.2UH CHOKE IS GIVEN AT B, THE COLOR BANDS FOR A 330UH INDUCTOR ARE ILLUSTRATED

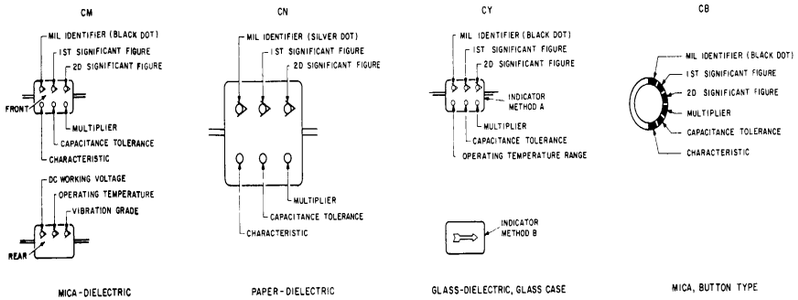
TABLE 2
COLOR CODING FOR TUBULAR ENCAPSULATED R F CHOKES

COLOR	SIGNIFICANT FIGURE	MULTIPLIER	INDUCTANCE TOLERANCE (PERCENT)
BLACK	0	1	
BROWN	1	10	1
RED	2	100	2
ORANGE	3	1,000	3
YELLOW	4		
GREEN	5		
BLUE	6		
VIOLET	7		
GRAY	8		
WHITE	9		
NONE			20
SILVER			10
GOLD	DECIMAL POINT		5

MULTIPLIER IS THE FACTOR BY WHICH THE TWO COLOR FIGURES ARE MULTIPLIED TO OBTAIN THE INDUCTANCE VALUE OF THE CHOKE COIL

B COLOR CODE MARKING FOR MILITARY STANDARD INDUCTORS

CAPACITORS, FIXED, VARIOUS-DIELECTRICS, STYLES CM, CN, CY, AND CB

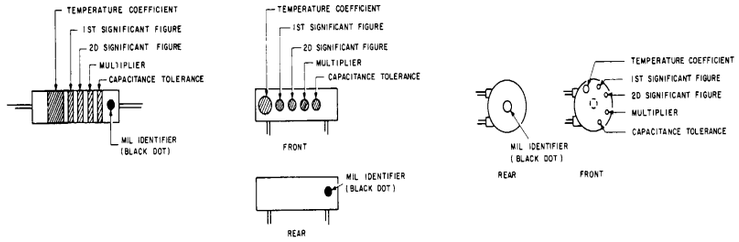


MICA-DIELECTRIC

PAPER-DIELECTRIC

GLASS-DIELECTRIC, GLASS CASE

MICA, BUTTON TYPE



AXIAL LEAD

RADIAL LEAD

DISK-TYPE

C COLOR CODE MARKING FOR MILITARY STANDARD CAPACITORS

TABLE 3 — FOR USE WITH STYLES CM, CN, CY AND CB

COLOR	MIL ID	1ST SIG FIG	2D SIG FIG	MULTIPLIER[1]	CAPACITANCE TOLERANCE				CHARACTERISTIC[2]			DC WORKING VOLTAGE	OPERATING TEMP RANGE	VIBRATION GRADE
					CM	CN	CY	CB	CM	CN	CB	CM	CY, CM	CM
BLACK	CM CY CB	0	0	1			±20%	±20%		A			-55°TO+70°C	10-55 HZ
BROWN		1	1	10					B	E	B			
RED		2	2	100	±2%		±2%	±2%	C				-55°TO+85°C	
ORANGE		3	3	1,000		±30%			D		D	300	"	
YELLOW		4	4	10,000					E				-55°TO+125°C	10-2,000HZ
GREEN		5	5		±5%				F			500		
BLUE		6	6										-55°TO+150°C	
PURPLE (VIOLET)		7	7											
GRAY		8	8											
WHITE		9	9											
GOLD				0.1			±5%	±5%						
SILVER	CN			0.01	±10%	±10%	±10%	±10%						

TABLE 4 — TEMPERATURE COMPENSATING, STYLE CC

COLOR	TEMPERATURE COEFFICIENT[3]	1ST SIG FIG	2D SIG FIG	MULTIPLIER[1]	CAPACITANCE TOLERANCE		MIL ID
					CAPACITANCES OVER 10 UUF	CAPACITANCES 10 UUF OR LESS	
BLACK	0	0	0	1		±2.0 UUF	CC
BROWN	-30	1	1	10	±1%		
RED	-80	2	2	100	±2%	±0.25 UUF	
ORANGE	-150	3	3	1,000			
YELLOW	-220	4	4				
GREEN	-330	5	5		±5%	±0.5 UUF	
BLUE	-470	6	6				
PURPLE (VIOLET)	-750	7	7				
GRAY		8	8	0.01*			
WHITE		9	9	0.1*	±10%		
GOLD	+100			0.1		±1.0 UUF	
SILVER				0.01			

1 THE MULTIPLIER IS THE NUMBER BY WHICH THE TWO SIGNIFICANT (SIG) FIGURES ARE MULTIPLIED TO OBTAIN THE CAPACITANCE IN UUF

2 LETTERS INDICATE THE CHARACTERISTICS DESIGNATED IN APPLICABLE SPECIFICATIONS MIL-C-5, MIL-C-25D, MIL-C-11272B, AND MIL-C-10950C RESPECTIVELY

3 LETTERS INDICATE THE TEMPERATURE RANGE AND VOLTAGE-TEMPERATURE LIMITS DESIGNATED IN MIL-C-11015D

4 TEMPERATURE COEFFICIENT IN PARTS PER MILLION PER DEGREE CENTIGRADE

* OPTIONAL CODING WHERE METALLIC PIGMENTS ARE UNDESIRABLE

ESC-FM 913 73

Figure FO-1. Color code markings for MIL-STD resistors and capacitors.

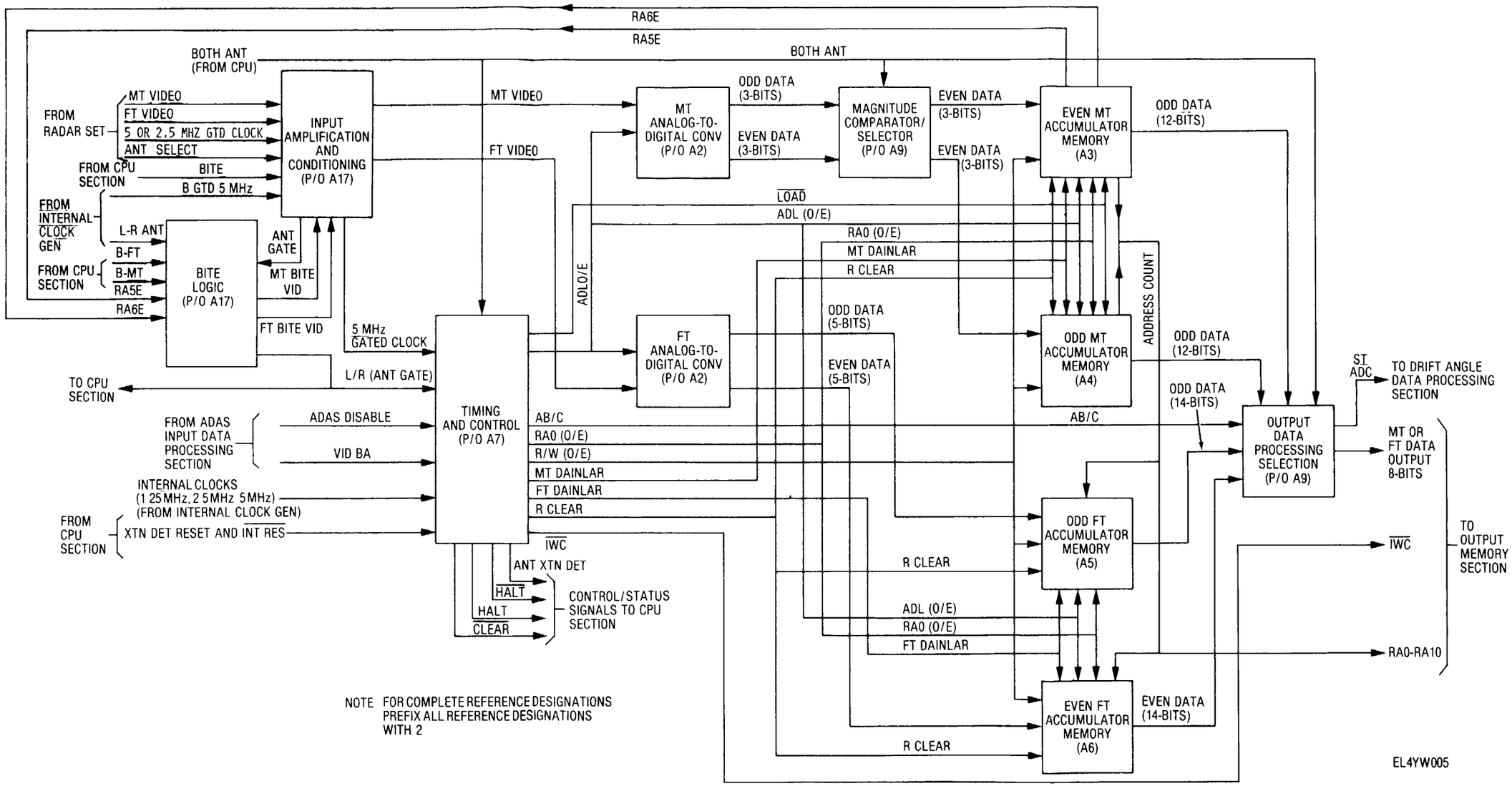


Figure FO-2. Video input data processing functional block diagram.

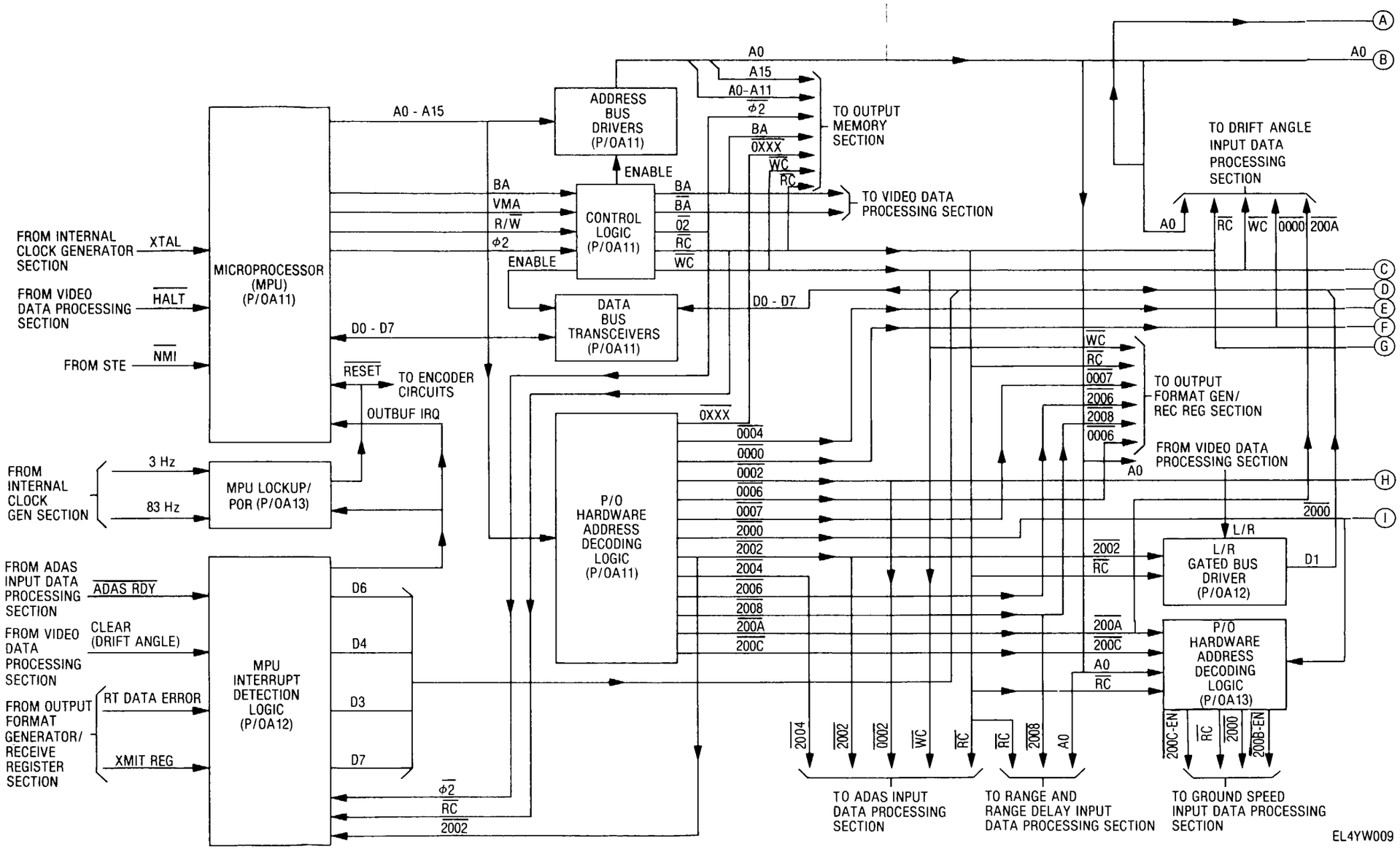


Figure FO-3. Central processing unit (CPU) functional block diagram (sheet 1 of 2).

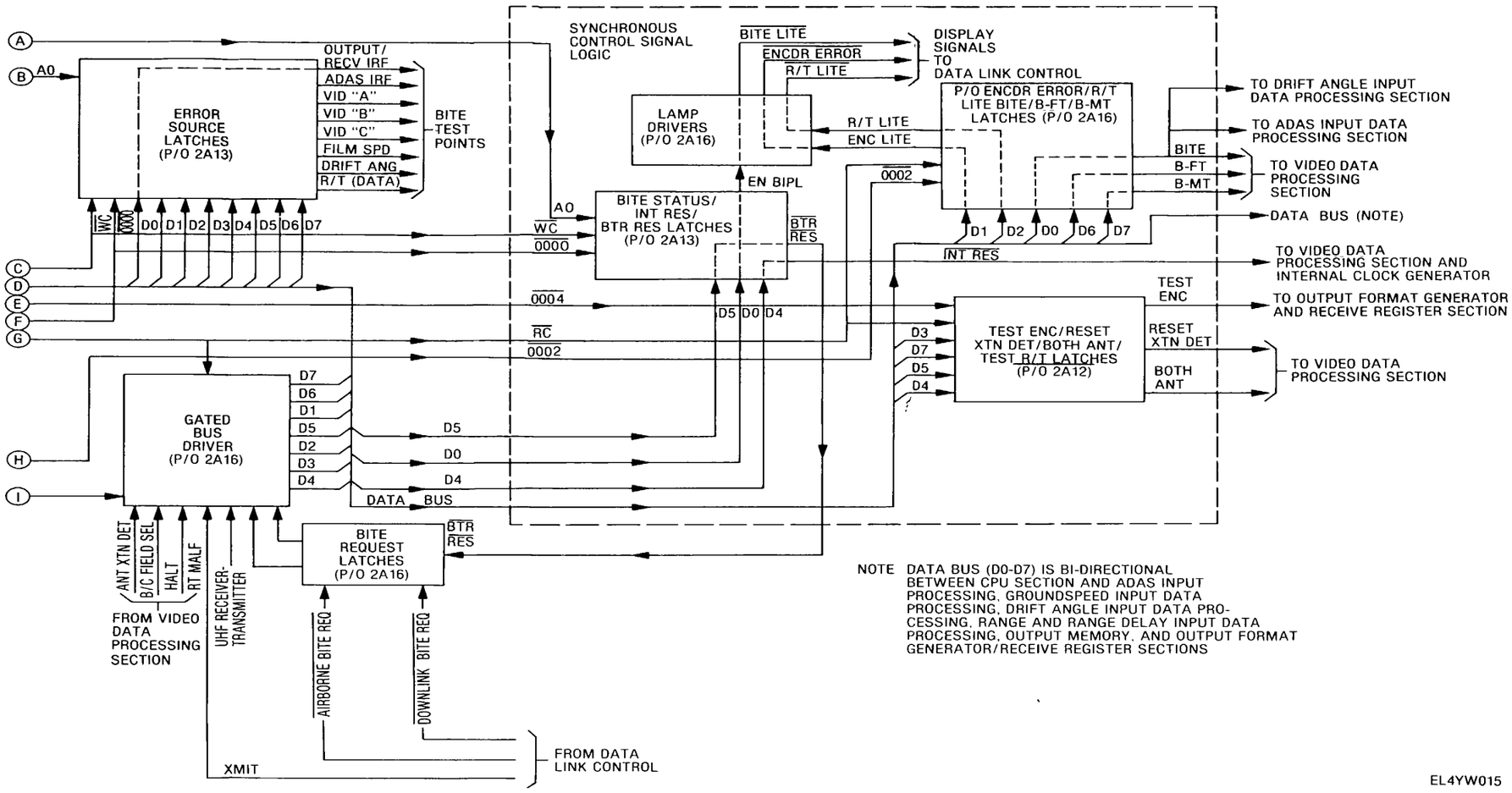


Figure FO-3. Central processing unit (CPU) functional block diagram (sheet 2 of 2).

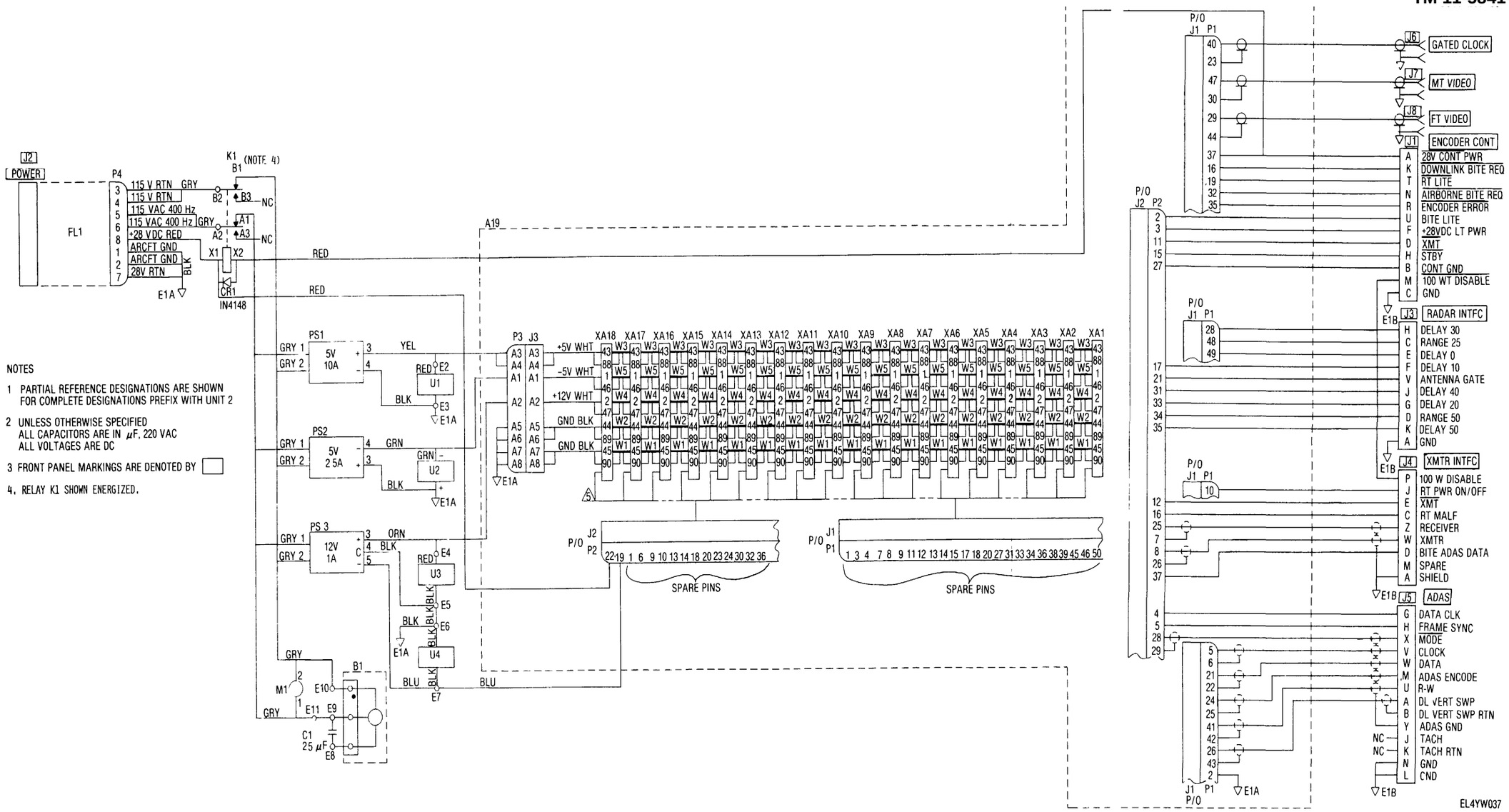


Figure FO-4. Encoder schematic diagram.

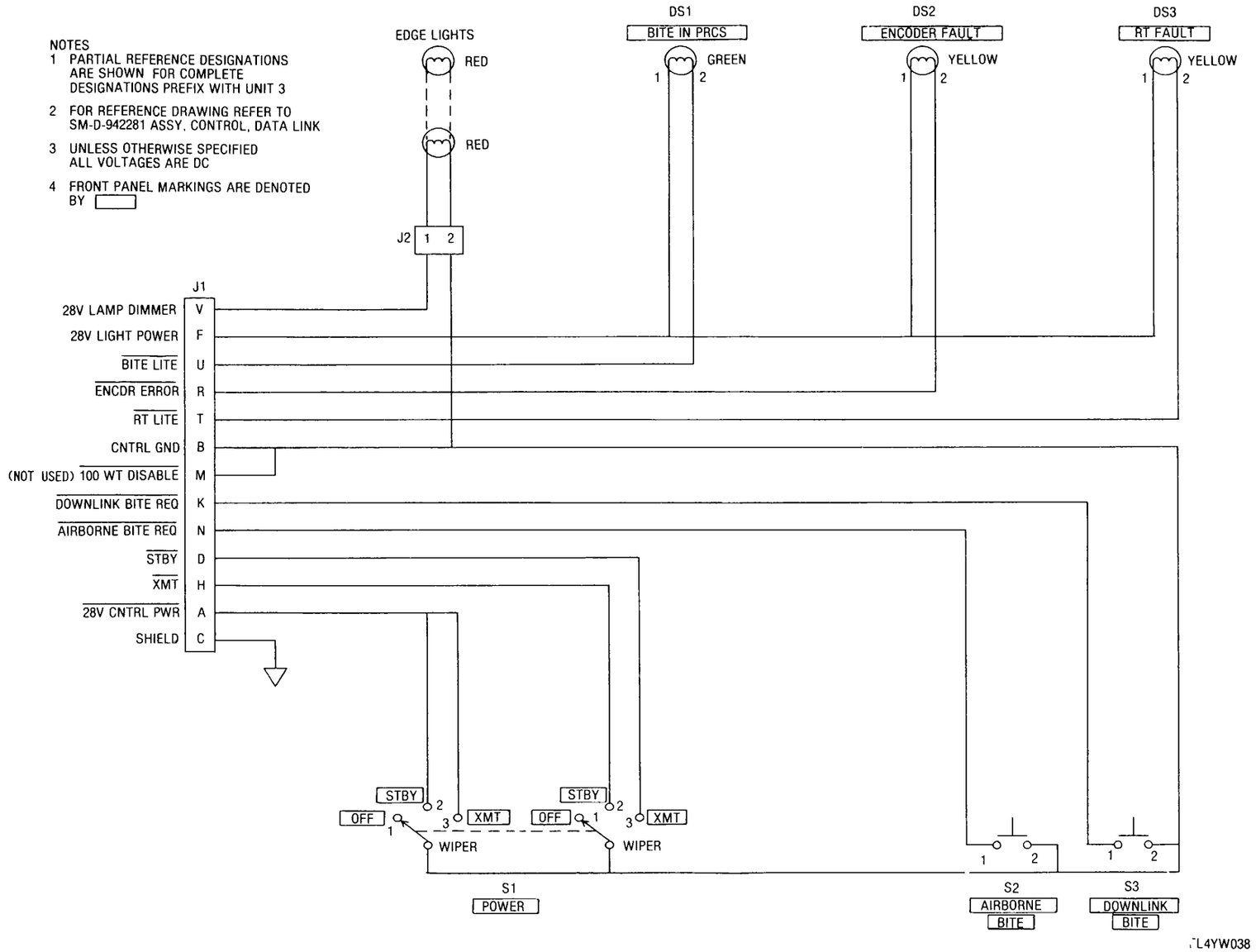


Figure FO-5. Data link control schematic diagram.

By Order of the Secretary of the Army

EDWARD C. MEYER
General, United States Army
Official: *Chief of Staff*

J.C. PENNINGTON
Major General, United States Army
The Adjutant General

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IN THIS SPACE TELL WHAT IS WRONG AND WHAT SHOULD BE DONE ABOUT IT:

PRINTED NAME, GRADE OR TITLE, AND TELEPHONE NUMBER

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DA FORM 1 JUL 79 2028-2

PREVIOUS EDITIONS ARE OBSOLETE.

P.S.—IF YOUR OUTFIT WANTS TO KNOW ABOUT YOUR RECOMMENDATION MAKE A CARBON COPY OF THIS AND GIVE IT TO YOUR HEADQUARTERS.

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